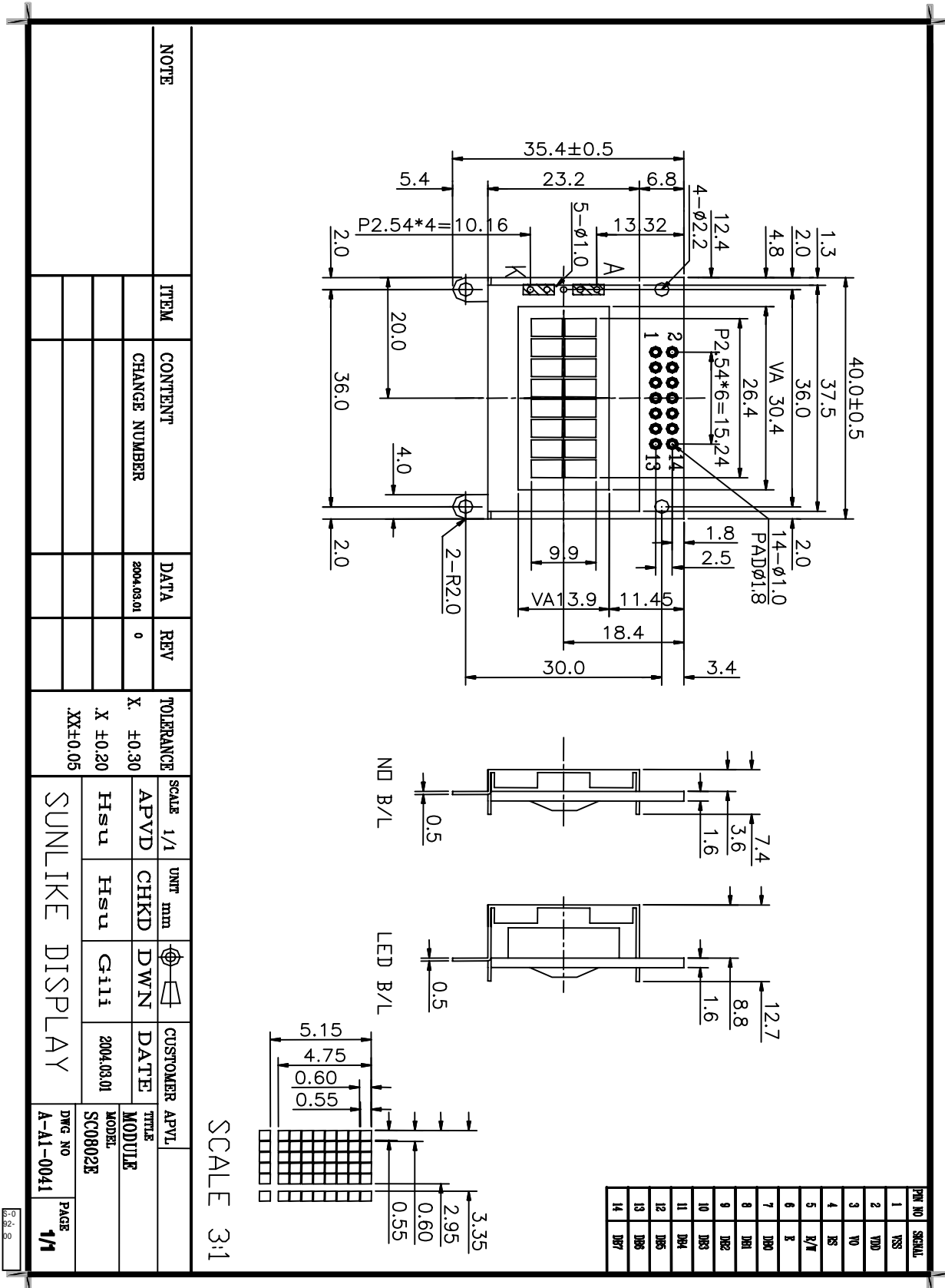


## GENERAL SPECIFICATION

ITEM	DESCRIPTION				
Product No	SC0802EBNB-XA-GB-G				
LCD Type	<input type="checkbox"/> STN Gray Positive	<input type="checkbox"/> STN Yellow Green Positive		STN Blue Negative	
	<input type="checkbox"/> TN Negative		<input type="checkbox"/> TN Positive		
	<input type="checkbox"/> FSTN Negative White & Black		<input type="checkbox"/> FSTN Positive Black & White		
Rear Polarizer	<input type="checkbox"/> Reflective		<input type="checkbox"/> Transflective		Transmissive
Backlight Type	<input type="checkbox"/> NO B/L	LED		<input type="checkbox"/> CCFL	<input type="checkbox"/> EL
Backlight Color	<input type="checkbox"/> Yellow Green	<input type="checkbox"/> Green	Red	<input type="checkbox"/> White	<input type="checkbox"/> Blue Green
View Direction	6 O'clock			<input type="checkbox"/> 12 O'clock	
Temperature Range	Normal			<input type="checkbox"/> Wide	
Frame	Black			<input type="checkbox"/> Silver	

### TO BE VERY CAREFUL !

The LCD driver ICs are made by CMOS process, which are very easy to be damaged by static charge, make sure the user is grounded when handling the LCM.



NOTE	ITEM	CONTENT	DATA	REV	TOLERANCE	SCALE	UNITS	CHKD	DWN	DATE	CUSTOMER	APVLT	TITLE	MODEL	DWG NO	PAGE
		CHANGE NUMBER	2004.03.01	0	X ±0.30 X ±0.20 .XX±0.05	1/1	mm	Hsu	G-111	2004.03.01			MODULE	SC0802E	A-A1-0041	1/1
SUNLIKE DISPLAY																

## ABSOLUTE MAXIMUM RATING

### (1) Electrical Absolute Ratings

Item	Symbol	Min.	Max.	Unit	Note
Power Supply for Logic	$V_{DD}-V_{SS}$	-0.3	7.0	Volt	
Power Supply for LCD	$V_{DD}-V_O$	-0.3	10.0	Volt	
Input Voltage	$V_I$	-0.3	$V_{DD}$	Volt	
LED Power Dissipation	$P_{AD}$	-	345	mW	
LED Forward current	$I_{AF}$	-	75	mA	
LED Reverse Voltage	$V_R$	-	8	V	

### (2) Environmental Absolute Maximum Ratings

Item	Normal Temperature				Wide Temperature			
	Operating		Storage		Operating		Storage	
	Min,	Max.	Min,	Max.	Min,	Max.	Min,	Max.
Ambient Temperature	0	+50	-20	+70	-20	+70	-30	+80
Humidity(without condensation)	Note 2,4		Note 3,5		Note 4,5		Note 4,6	

Note 2  $T_a = 50$  : 80% RH max

$T_a > 50$  : Absolute humidity must be lower than the humidity of 85%RH at 50

Note 3  $T_a$  at -20 will be <48hrs at 70 will be <120hrs when humidity is higher than 70%.

Note 4 Background color changes slightly depending on ambient temperature. This phenomenon is reversible.

Note 5  $T_a = 70$  : 75RH max

$T_a > 70$  : absolute humidity must be lower than the humidity of 75%RH at 70

Note 6  $T_a$  at -30 will be <48hrs, at 80 will be <120hrs when humidity is higher than 70%.

## ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Min.	Typ	Max.	Unit	note
Power Supply for Logic	$V_{DD}-V_{SS}$	-	4.5	5.0	5.5	Volt	
Input Voltage	$V_{IL}$	L level	0	-	0.6	Volt	
	$V_{IH}$	H level	2.2	-	$V_{DD}$	Volt	
LCM Recommend LCD Module Driving Voltage	$V_{DD}-V_O$	Ta = 0	-	-	-	Volt	
		Ta = 25	4.2	4.5	4.8		
		Ta = 50	-	-	-		
Power Supply Current for LCM	$I_{DD}$	$V_{DD}=5.0V$ $V_{DD}-V_O=4.5V$	-	1.5	2.0	mA	
LED Forward Voltage	$V_F$	If = 50 mA	-	4.1	4.6	Volt	
LED Forward Current	$I_F$	-	-	50	-	mA	
LED Reverse Current	$I_R$	VR=8V	-	-	0.2	mA	

## OPTICAL CHARACTERISTICS

Item	Symbol	Condition	Min.	Typ	Max.	Unit	note
Viewing angle range	f(12 o'clock)	When Cr 1.4	-	20	-	Degree	9,10
	b(6 o'clock)		-	40	-		
	l(9 o'clock)		-	30	-		
	r(3 o'clock)		-	30	-		
Rise Time	Tr	$V_{DD}-V_O=4.5V$ Ta=25		100	200	mS	
Fall Time	Tf			200	350		
Frame frequency	Frm		-	64	-	Hz	8,10
Contrast	Cr		-	3.0	-		7
The Brightness Of Backlight	L	IF=50 mA	100	120	-	cd/m <sup>2</sup>	
Peak Emission Wavelength	P		600	605	610	nm	

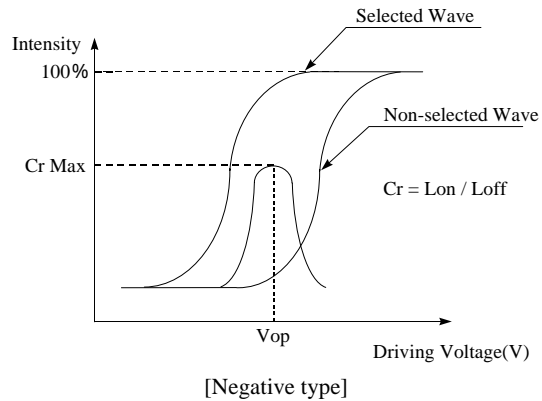
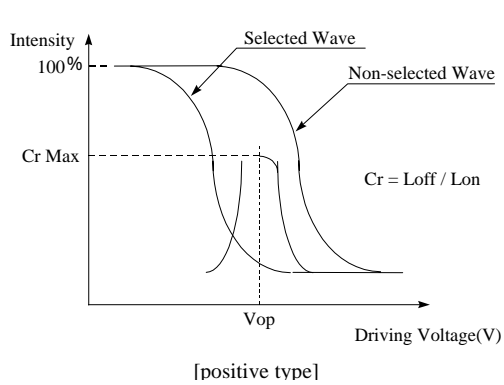
## MECHANICAL SPECIFICATION

ITEM	DESCRIPTION
Product No.	SC0802E
Module Size	40.0(W)×35.4(H)×7.4(LED12.7) max(D)
Viewing Area	30.4(W)mm×13.9(H)mm
Dot Size	0.55(W)mm×0.55(H)mm
Dot Pitch	0.60(W)mm×0.60(H)mm
Display Format	8 characters (W)×2 lines (H)
Duty Ratio	1/16 Duty
Controller	ST7066U or Equivalent

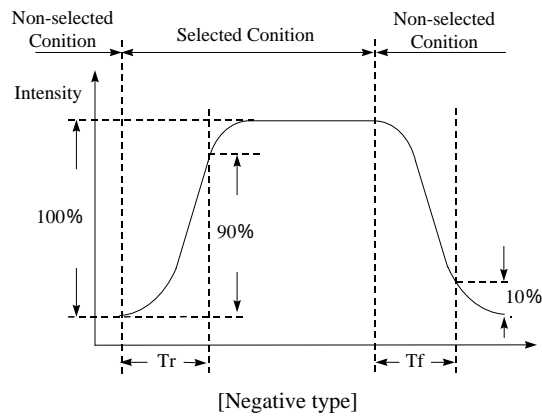
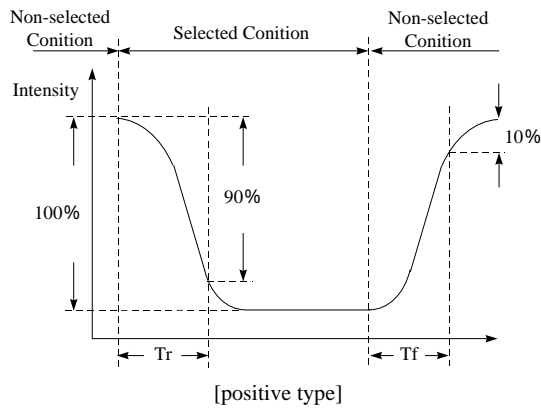
## INTERFACE PIN ASSIGNMENT

Pin No.	Pin Out	Level	Description
1	VSS	0V	Power Supply Ground
2	VDD	5V	Power Supply Voltage
3	Vo	---	Contrast Adj
4	RS	H/L	Register Select
5	R/W	H/L	Read / Write
6	E	H,H L	Enable Signal
7	DB0	H/L	Data Bit 0
8	DB1	H/L	Data Bit 1
9	DB2	H/L	Data Bit 2
10	DB3	H/L	Data Bit 3
11	DB4	H/L	Data Bit 4
12	DB5	H/L	Data Bit 5
13	DB6	H/L	Data Bit 6
14	DB7	H/L	Data Bit 7

### [Note 7] Definition of Operation Voltage (Vop)



### [Note 8] Definition of Response Time (Tr, Tf)



### Conditions:

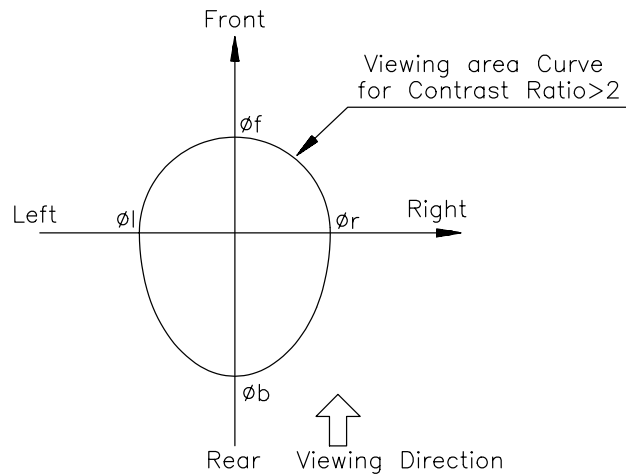
**Operating Voltage : Vop**

**Frame Frequency : 64 Hz**

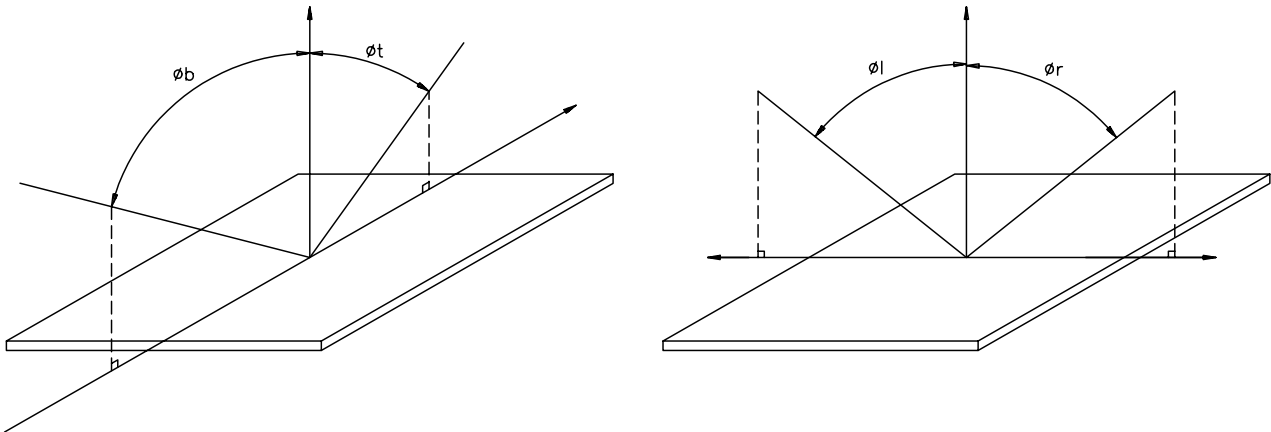
**Viewing Angle ( , ): 0°, 0°**

**Driving Wave form : 1/N duty, 1/a bias**

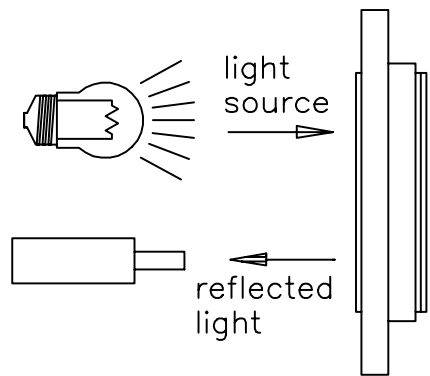
### [Note 9] Definition of Viewing Direction



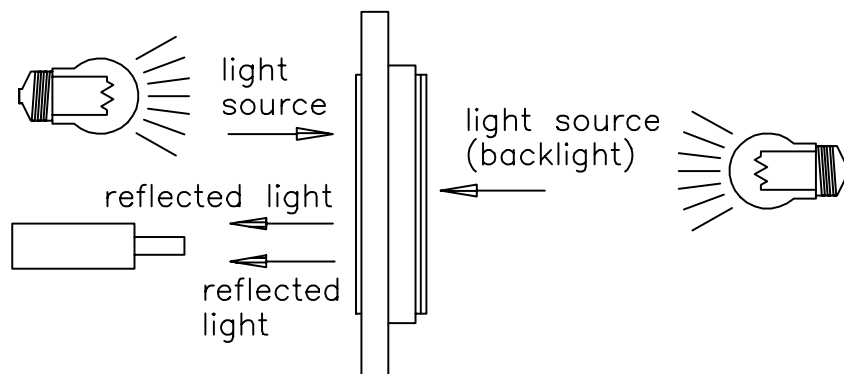
**[Note 10] Definition of viewing angle**



**[Note 11] Description of Measuring Equipment**

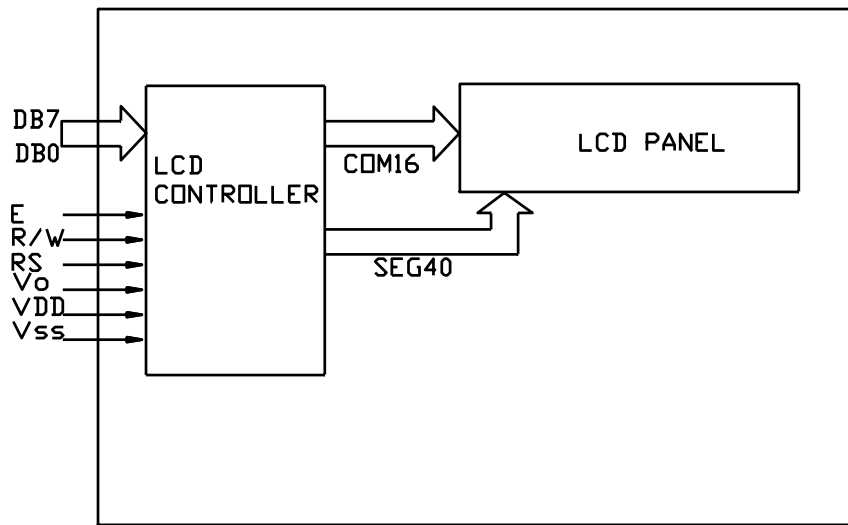


Reflective type

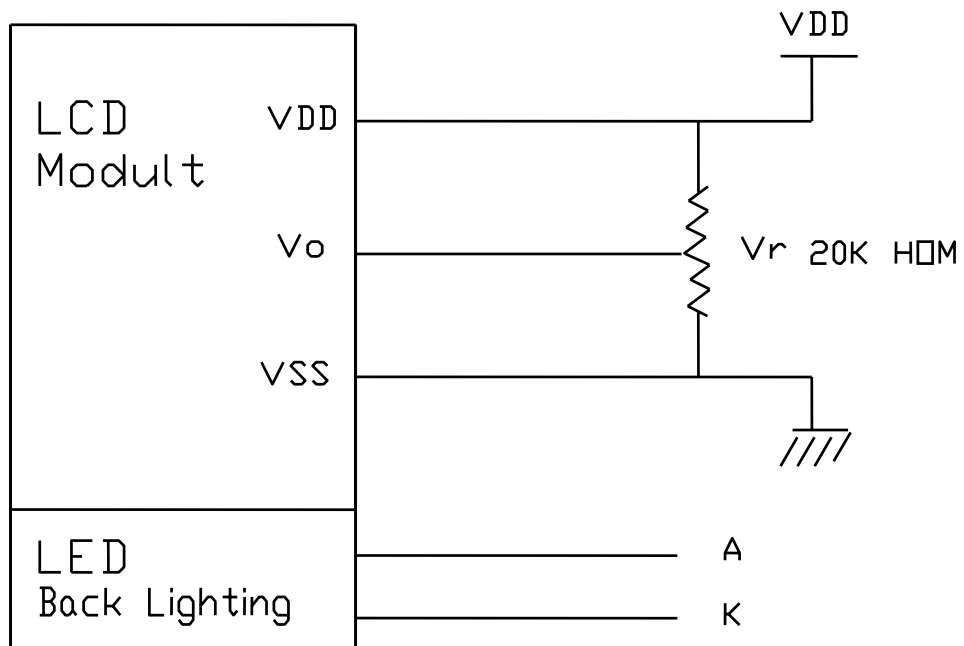


Transflective type

## BLOCK DIAGRAM



## POWER SUPPLY





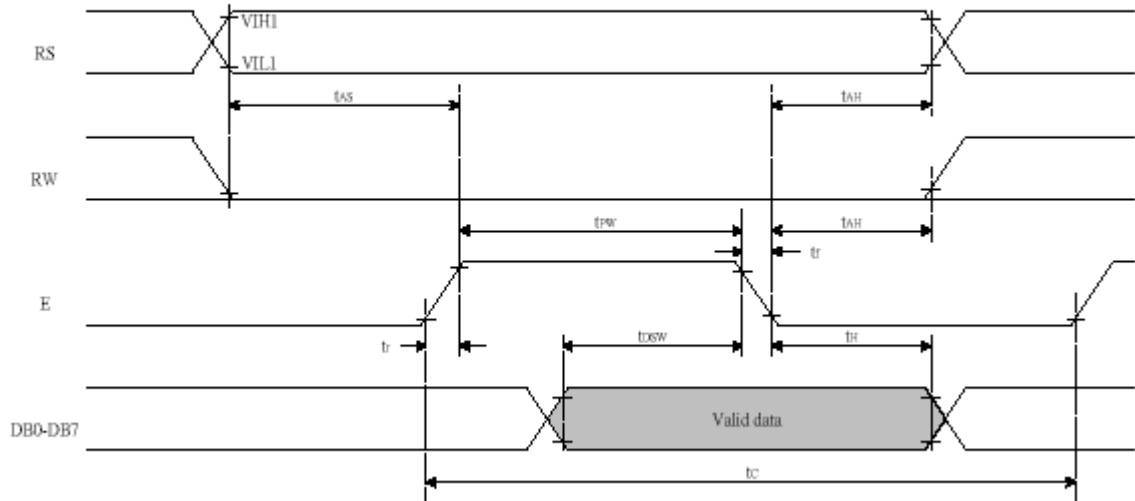
## TIMING CHARACTERISTICS

TA=25 ,VCC=5V

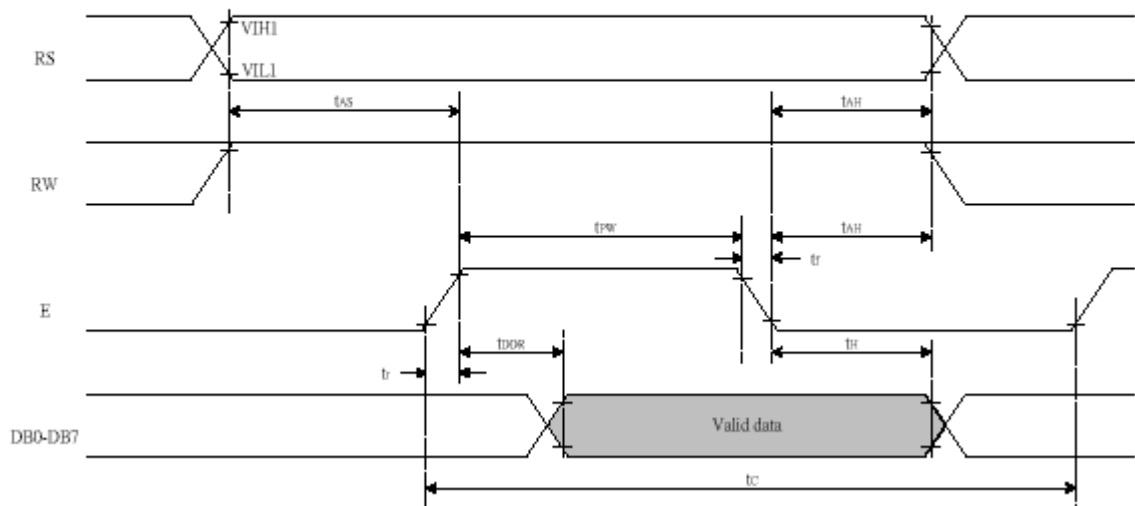
Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
<i>Internal Clock Operation</i>						
f <sub>osc</sub>	OSC Frequency	R = 91KΩ	190	270	350	KHz
<i>External Clock Operation</i>						
f <sub>EX</sub>	External Frequency	-	125	270	410	KHz
	Duty Cycle	-	45	50	55	%
T <sub>R</sub> ,T <sub>F</sub>	Rise/Fall Time	-	-	-	0.2	μs
<i>Write Mode (Writing data from MPU to ST7066U)</i>						
T <sub>C</sub>	Enable Cycle Time	Pin E	1200	-	-	ns
T <sub>PW</sub>	Enable Pulse Width	Pin E	140	-	-	ns
T <sub>R</sub> ,T <sub>F</sub>	Enable Rise/Fall Time	Pin E	-	-	25	ns
T <sub>AS</sub>	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T <sub>AH</sub>	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T <sub>DSW</sub>	Data Setup Time	Pins: DB0 - DB7	40	-	-	ns
T <sub>H</sub>	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
<i>Read Mode (Reading Data from ST7066U to MPU)</i>						
T <sub>C</sub>	Enable Cycle Time	Pin E	1200	-	-	ns
T <sub>PW</sub>	Enable Pulse Width	Pin E	140	-	-	ns
T <sub>R</sub> ,T <sub>F</sub>	Enable Rise/Fall Time	Pin E	-	-	25	ns
T <sub>AS</sub>	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T <sub>AH</sub>	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T <sub>DDR</sub>	Data Setup Time	Pins: DB0 - DB7	-	-	100	ns
T <sub>H</sub>	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns

## Read/Write Timing Chart

- Writing data from MPU to ST7066U



- Reading data from ST7066U to MPU



## Commands

Instruction	Instruction Code										Description	Description Time (270KHz)	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear Display	0	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.52 ms
Return Home	0	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.52 ms
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 us
Display ON/OFF	0	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	37 us
Cursor or Display Shift	0	0	0	0	0	0	1	S/C	R/L	x	x	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	37 us
Function Set	0	0	0	0	0	1	DL	N	F	x	x	DL:interface data is 8/4 bits N:number of line is 2/1 F:font size is 5x11/5x8	37 us
Set CGRAM address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0		Set CGRAM address in address counter	37 us
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Set DDRAM address in address counter	37 us
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 us
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0		Write data into internal RAM (DDRAM/CGRAM)	37 us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0		Read data from internal RAM (DDRAM/CGRAM)	37 us

**Note:**

Be sure the ST7066U is not in the busy state (BF = 0) before sending an instruction from the MPU to the ST7066U. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Instruction Table for the list of each instruction execution time.

---

## Reset Function

### Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the IC when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 40 ms after VCC rises to 4.5 V.

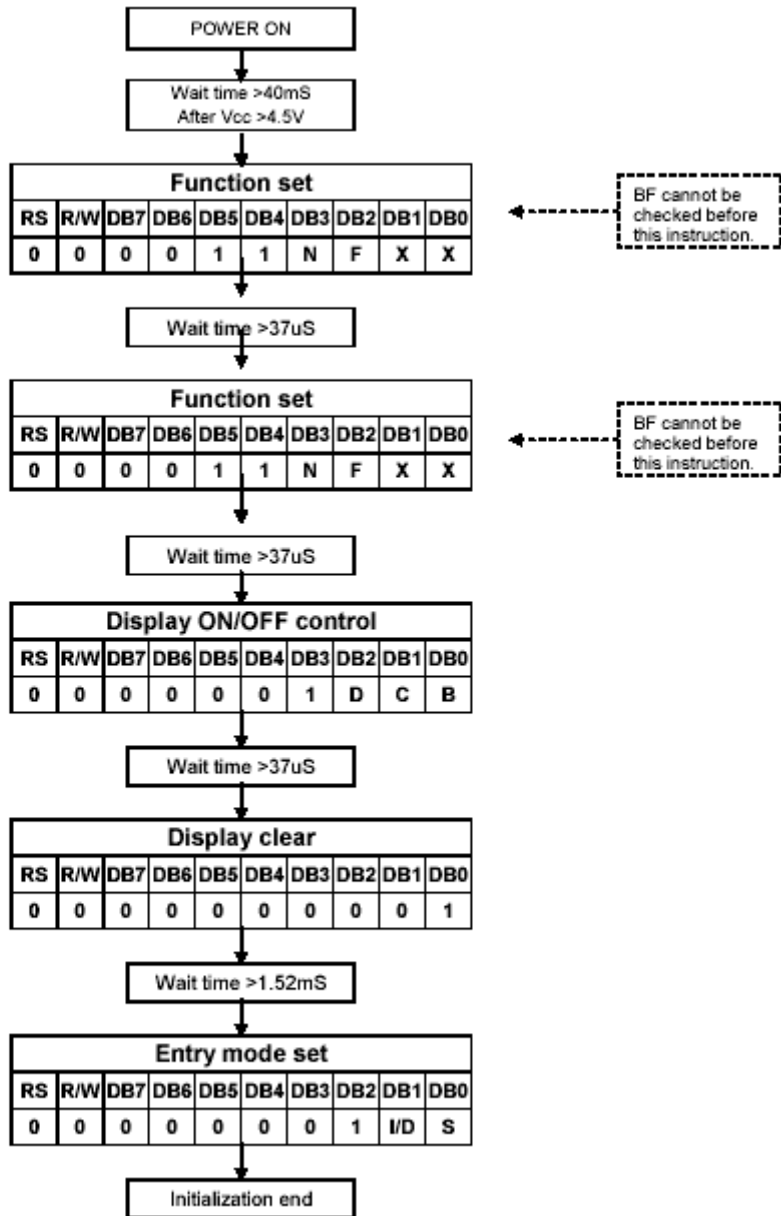
1. Display clear
2. Function set:
  - DL = 1; 8-bit interface data
  - N = 0; 1-line display
  - F = 0; 5x8 dot character font
3. Display on/off control:
  - D = 0; Display off
  - C = 0; Cursor off
  - B = 0; Blinking off
4. Entry mode set:
  - I/D = 1; Increment by 1
  - S = 0; No shift

#### Note:

If the electrical characteristics conditions listed in the table Power Supply Conditions are not met, the internal reset circuit will not operate normally and will fail to initialize the IC. For such a case, initialization must be performed by the MPU as explain by the following figures.

## Initializing by Instruction

8 bit Interface( fosc =270KHZ)



## DD RAM ADDRESSING

### For 10\*4 Display

	1	2	3	4	5	6	7	8	9	10
Character	00	01	02	03	04	05	06	07	08	09
DD RAM	40	41	42	43	44	45	46	47	48	49
Address	0A	0B	0C	0D	0E	0F	10	11	12	13
	5A	5B	5C	5D	5E	5F	50	51	52	53

### For 16\*1 Display

Character	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM	00	01	02	03	04	05	06	07	40	41	42	43	44	45	46	47
Address																

### For 16\*2 or 8\*2 Display

Character	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM	00	01	02	03	04	05	06	07	8	9	0A	0B	0C	0D	0E	0F
Address	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

### For 16\*4 Display

Character	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
Address	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F

### For 20\*2 Display

Character	1	2	3	4	5	6	7	8	9	10	---	---	17	18	19	20
DD RAM	00	01	02	03	04	05	06	07	08	09	---	---	10	11	12	13
Address	40	41	42	43	44	45	46	47	48	49	---	---	50	51	52	53

### For 20\*4 Display

	1	2	3	4	5	6	7	8	9	10	---	---	17	18	19	20
Character DD RAM Address	00	01	02	03	04	05	06	07	08	09	---	---	10	11	12	13
	40	41	42	43	44	45	46	47	48	49	---	---	50	51	52	53
	14	15	16	17	18	19	1A	1B	1C	1D	---	---	24	25	26	27
	54	55	56	57	58	59	5A	5B	5C	5D	---	---	64	65	66	67

### For 40\*2 Display

	1	2	3	4	5	6	7	8	9	10	---	---	37	38	39	40
Character DD RAM Address	00	01	02	03	04	05	06	07	08	09	---	---	24	25	26	27
	40	41	42	43	44	45	46	47	48	49	---	---	64	65	66	67

### For 40\*4 Display

	E	1	2	3	4	5	6	7	8	9	10	---	---	37	38	39	40
Character DD RAM Address	E1	00	01	02	03	04	05	06	07	08	09	---	---	24	25	26	27
		40	41	42	43	44	45	46	47	48	49	---	---	64	65	66	67
	E2	00	01	02	03	04	05	06	07	08	09	---	---	24	25	26	27
		40	41	42	43	44	45	46	47	48	49	---	---	64	65	66	67

## CG RAM MAPPING

Character Code (DD RAM data)								CG RAM Address						Character Patterns (CG RAM data)																																																
7	6	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0																																									
High				Low				High			Low			High				Low																																												
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1	1	1	1	1																																																										
0	0	0	0	0																																																										



CHARACTER FONT TABLE

Upper 4 bit Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL				0	1	2	3	4					一	夕	三	四
LLLH			!	1	A	Q	3	4			。	ア	チ	△	当	9
LLHL			"	2	B	R	6	7			「	イ	ウ	×	目	日
LLHH			#	3	D	S	5	6			」	ウ	テ	毛	三	8
LHLL			\$	4	D	T	d	t			ノ	工	ト	カ	以	2
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