WINSTAR Display

IC SPECIFICATION

Model No:

WS0010

MODLE NO：

RECORDS OF REVISION			DOC. FIRST ISSUE
VERSION	DATE	REVISED PAGE NO.	SUMMARY
0	2011.02.22		First issue
A	2011.05.30	21	Correct INITIALIZATION BY INSTRUCTION

FUNCTION DESCRIPTION

REGISTERS

WS0010 provides two types of 8-bit registers, namely: Instruction Register (IR) and Data Register (DR). The register is selected using the RS Pin. When the RS pin is set to "0", the Instruction Register Type is selected. When RS pin is set to "1", the Data Register Type is selected. Please refer to the table below.

RS	R/WB	Operation
0	0	Instruction register write as an internal operation.
0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	Data register write as an internal operation (DR to DDRAM or CGRAM)
1	1	Data register read as an internal operation (DDRAM or CGRAM to DR)

INSTRUCTION REGISTER (IR)

The Instruction Register is used to store the instruction code (i.e. Display Clear, Cursor Home and others), Display Data RAM (DDRAM) Address, and the Character Generator RAM (CGRAM) Address. Instruction register can only be written from the MPU.

DATA REGISTER (DR)

The Data Register is used as a temporary storage for data that are going to be written into the DDRAM or CGRAM as well as those data that are going to be read from the DDRAM or CGRAM.

BUSY FLAG (BF)

The Busy Flag is used to determine whether WS0010 is idle or internally operating. When WS0010 is performing some internal operations, the Busy Flag is set to "1". Under this condition, the no other instruction will not be accepted. When RS Pin is set to "0" and R/WB Pin is set to "1", the Busy Flag will be outputted to the DB7 pin.

When WS0010 is idle or has completed its previous internal operation, the Busy Flag is set to "0". The next instruction can now be processed or executed.

ADDRESS COUNTER (AC)

The address counter is used to assign the Display Data RAM (DDRAM) Address and the Character Generator RAM (CGRAM) Address. When Address information is written into the Instruction Register (IR), this Address information is sent from the Instruction Register to the Address Counter. At the same time, the nature of the Address (either CGRAM or DDRAM) is determined by the instruction.
After writing into or reading from the DDRAM or CGRAM, the Address Counter is automatically increased or decreased by 1 (for Write or Read Function). It must be noted that when the RS pin is set to "0" and R/WB is set to "1", the contents of the Address Counter are outputted to the pins -- DB0 to DB6.

DISPLAY DATA RAM (DDRAM)

The Display Data RAM (DDRAM) is used to store the Display Data which is represented as 8-bit character code. The Display Data RAM supports an extended capacity of 128 x 8-bits or 128 characters.

The Display Data RAM Address (ADD) is set in the Address Counter as a hexadecimal.

	High Order Bits			Low Order Bits			
Address Counter (hex)	AC6	AC5	AC4	AC3	AC2	AC1	AC0

An example of a DDRAM Address=39 is given below.

DDRAM Address: 39						
AC6	AC5	AC4	AC3	AC2	AC1	AC0
0	1	1	1	0	0	1

1-LINE DISPLAY (N=0)

When the number of characters displayed is less than 128, the first character is displayed at the head position. The relationship between the DDRAM Address and position on the OLED Panel is shown below.

Display Position (digit)	1	2	3	4	……	126	127	128
DDRAM address (hexadecimal)	00	01	02	03	……	7D	7E	7F

For example, when only 8 characters are displayed in one Display Line, the relationship between the DDRAM Address and position on the OLED Panel is shown below.

Display Position	1	2	3	4	5	6	7	8
DDRAM address	00	01	02	03	04	05	06	07
Shift left	01	02	03	04	05	06	07	08
Shift right	7F	00	01	02	03	04	05	06

2-LINE DISPLAY (N=1)

Case 1: The Number of Characters displayed is less than 64 x 2 lines

When the number of characters displayed is less than 64 x 2 lines, then the first character of the first and second lines are displayed starting from the head. It is important to note that every line reserve 64 x8bits DDRAM space. 1st line is 00 to 3F,second line is 40 to 7F.Please refer the figure below.

Display Position	**1**	**2**	**3**	**4**	**…….**	**61**	**62**	**63**	**64**
DDRAM Address (hexadecimal)	00	01	02	03	…….	3C	3D	3E	3F
	40	41	42	43	…….	7C	7D	7E	7F

To illustrate, for 2-line x 20 characters display, the relationship between the DDRAM address and position of the OLED panel is shown below.

Display Position	**1**	**2**	**3**	**4**	**…….**	18	19	20
DDRAM address (hexadecimal)	00	01	02	03	**…….**	11	12	13
	40	41	42	43	**…….**	51	52	53
Shift left	01	02	03	04	**…….**	12	13	14
	41	42	43	44	**…….**	52	53	54
Shift right	3F	00	01	02	**…….**	10	11	12
	7F	40	41	42	**…….**	50	51	52

Case 2: 40-Character x 2 Lines Display

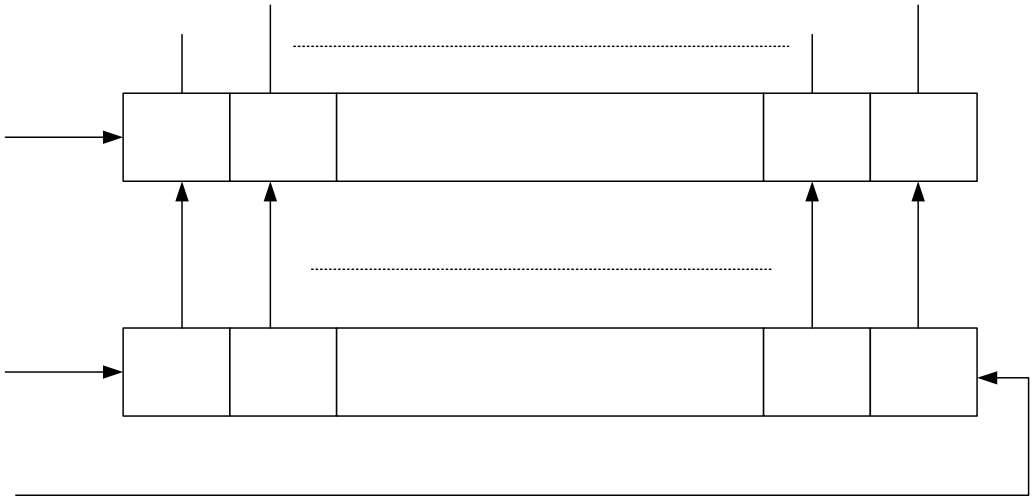
WS0010(Master) can be extended to display 40 characters x 2 lines by cascade the other WS0010(Slave). When there is a Display Shift operation, the DDRAM Address is also shifted. Please refer to the example below.

Display Position	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**….**	**37**	**38**	**39**	**40**
DDRAM address	00	01	02	03	04	05	06	07	08	09	0A	**….**	**24**	**25**	**26**	**27**
	40	41	42	43	44	45	46	47	48	49	4A	**….**	**64**	**65**	**66**	**67**
	WS0010 display (Master)								Cascade 2nd WS0010(Slave)							
Shift left	01	02	03	04	05	06	07	08	09	0A	0B	**….**	**25**	**26**	**27**	**28**
	41	42	43	44	45	46	47	48	49	4A	4B	**….**	**65**	**66**	**67**	**68**
Shift right	3F	00	01	02	03	04	05	06	07	08	09	**….**	**23**	**24**	**25**	**26**
	7F	40	41	42	43	44	45	46	47	48	49	**….**	**63**	**64**	**65**	**66**

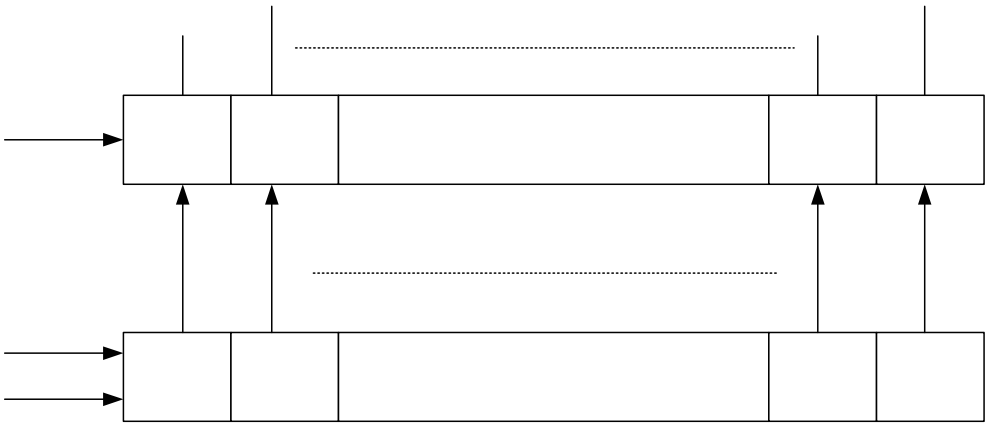
BIDIRECTIONAL SHIFT REGISTER BLOCK

This block shifts the serial data at the falling edge of CL. When SHL is set “H”, the data input from D is shifted from bit100 to bit1 (When WS0010 is “master” mode, D is output; When WS0010 is “slave” mode, D is input). When SHL is set “L”, the data input is shifted from bit1 to bit100.

Condition 1 : SHL=”H”



Condition 2 : SHL=”L



SG1

CHARACTER GENERATOR ROM (CGROM)

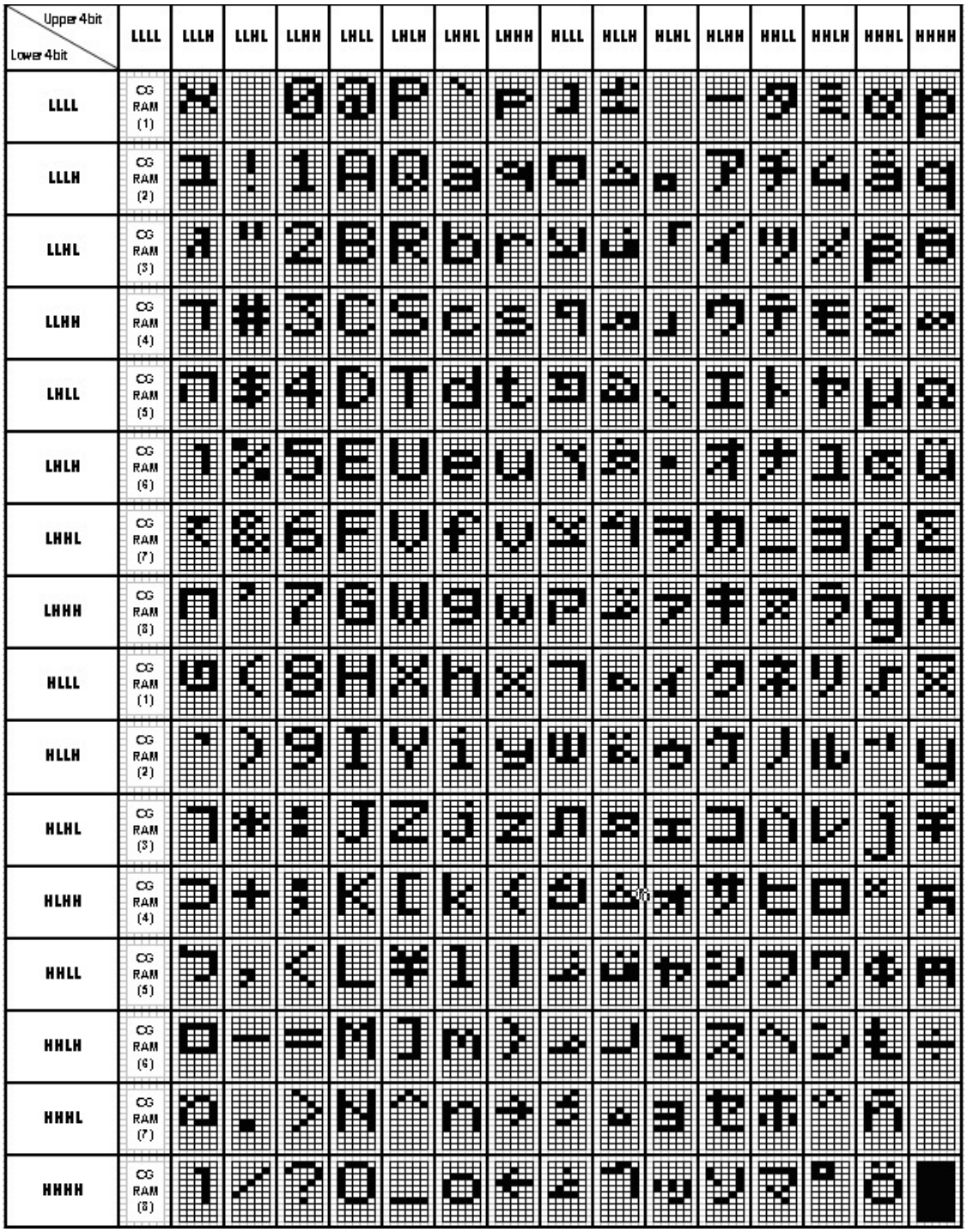
The Character Generator ROM (CGROM) is used to generate either 5 x 8 dots or 5 x 10 dots character patterns from 8-bit character codes.WS0010 build in four set of font tables as “Western European-I”, ”English Japanese”, “English Russian” and “Western European-II” . User can use software to select suitable font table **(Default “English Japanese”)**.

CHARACTER GENERATOR ROM (CGROM)

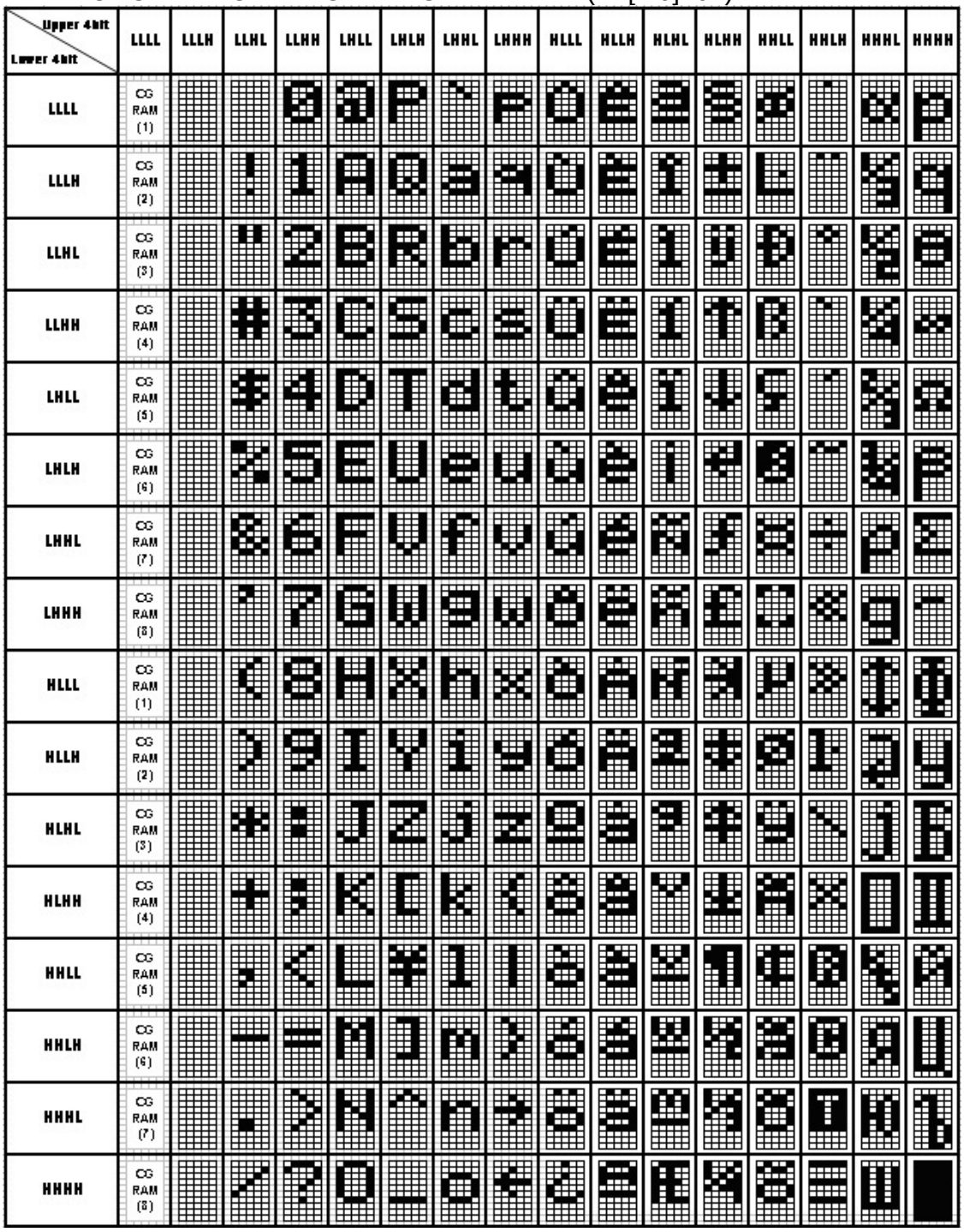
WS0010 provides three set of character font. Character font can be selected by programming FT.

ENGLISH_JAPANESE CHARACTER FONT TABLE(default FT[1:0]= 00)

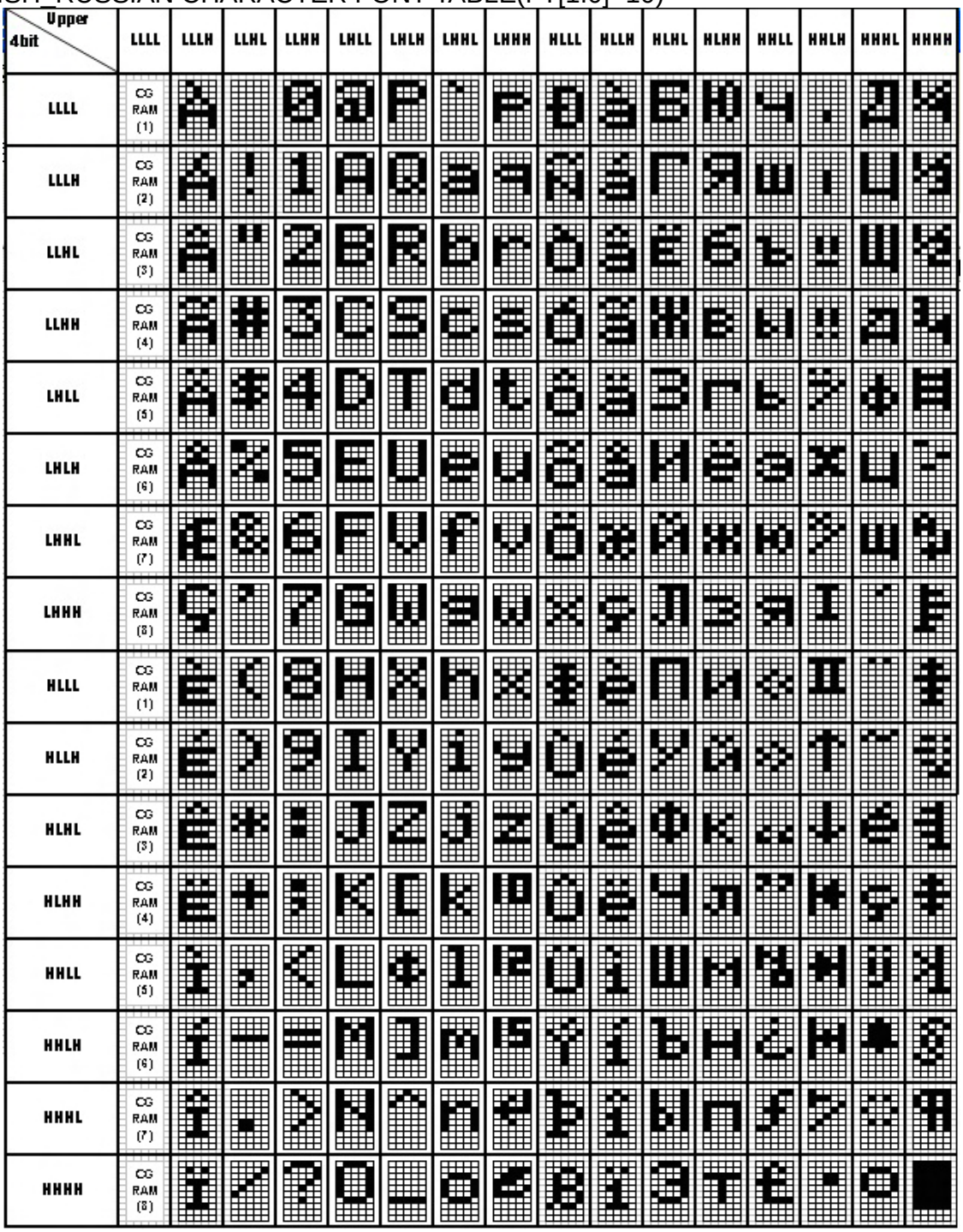
LAT


Upper 4bit
Lower 4bit
LLLL
LLLH
LLHL
LLHH
LHLL
LHLH
LHHL
LHHH
HLLL
HLLH
HLHL
HLHH
HHLL
HHLH
HHHL
HHHH
CG RAM (1)
CG RAM (2)
CG RAM (3)
CG RAM (4)
CG RAM (5)
CG RAM (6)
CG RAM (7)
CG RAM (8)

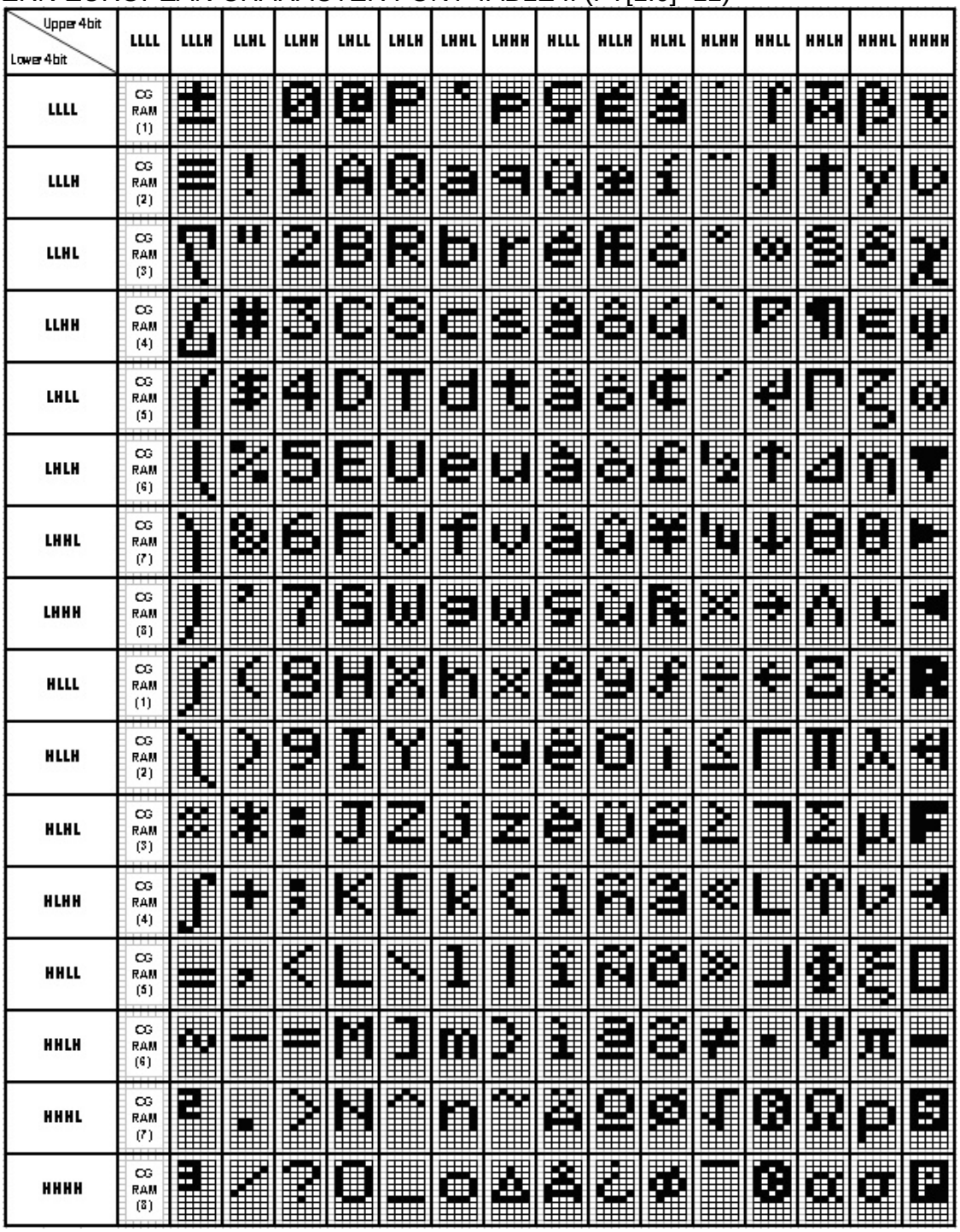
WESTERN EUROPEAN CHARACTER FONT TABLE I (FT[1:0]=01)



ENGLISH_RUSSIAN CHARACTER FONT TABLE(FT[1:0]=10)



WESTERN EUROPEAN CHARACTER FONT TABLE II (FT[1:0]=11)



CHARACTER GENERATOR RAM (CGRAM)

The Character Generator RAM (CGRAM) is used to generate either 5 x 8 dot or 5 x 10 dot character patterns. It can generate eight 5 x 8 dot character patterns or four 5 x 10 dot character patterns. The character patterns generated by the CGRAM can be rewritten. User-defined character patterns for the CGRAM are supported.

RELATIONSHIP BETWEEN CGRAM ADDRESS, DDRAM CHARACTER CODE AND CGRAM CHARACTER PATTERNS (FOR 5 X 8 DOT CHARACTER PATTERN)

Character Codes (DDRAM Data)									CGRAM Address							Character Patterns (CGRAM Data)								
7	6	5	4	3	2	1	0		5	4	3	2	1	0		7	6	5	4	3	2	1	0	
High						Low			High				Low			High						Low		
0	0	0	0	*	0	0	0		0	0	0	0	0	0		*	*	*	1	1	1	1	0	Character pattern 1
												0	0	1		*	*	*	1	0	0	0	1	
												0	1	0		*	*	*	1	0	0	0	1	
												0	1	1		*	*	*	1	1	1	1	0	
												1	0	0		*	*	*	1	0	1	0	0	
												1	0	1		*	*	*	1	0	0	1	0	
												1	1	0		*	*	*	1	0	0	0	1	
												1	1	1		*	*	*	0	0	0	0	0	Cursor Position
0	0	0	0	*	0	0	1		0	0	1	0	0	0		*	*	*	1	0	0	0	1	Character pattern 2
												0	0	1		*	*	*	0	1	0	1	0	
												0	1	0		*	*	*	1	1	1	1	1	
												0	1	1		*	*	*	0	0	1	0	0	
												1	0	0		*	*	*	1	1	1	1	1	
												1	0	1		*	*	*	0	0	1	0	0	
												1	1	0		*	*	*	0	0	1	0	0	
												1	1	1		*	*	*	0	0	0	0	0	Cursor position
0	0	0	0	*	. . . . .	. . . . .	. . . . .		. . . . .	. . . . .	. . . . .	. . . . .	. . . . .	. . . . .		*	*	*	. . . . .	. . . . .	. . . . .	. . . . .	. . . . .	Character pattern 3~7
0	0	0	0	*	1	1	1		1	1	1	0	0	0		*	*	*	0	0	0	0	0	Character pattern 8
												0	0	1		*	*	*	0	1	0	1	0	
												0	1	0		*	*	*	0	0	0	0	0	
												0	1	1		*	*	*	0	0	0	0	0	
												1	0	0		*	*	*	1	0	0	0	1	
												1	0	1		*	*	*	0	1	1	1	0	
												1	1	0		*	*	*	0	0	1	0	0	
												1	1	1		*	*	*	0	0	0	0	0	Cursor position

Notes:

1. * = Not Relevant
2. The character pattern row positions correspond to the CGRAM data bits -- 0 to 4, where bit 4 is in the left position.
3. Character Code Bits 0 to 2 correspond to the CGRAM Address Bits 3 to 5 (3 bits: 8 types)
4. If the CGRAM Data is set to "1", then the selection is displayed. If the CGRAM is set to "0", there no selection is made.
5. The CGRAM Address Bits 0 to 2 are used to define the character pattern line position. The 8th line is the cursor position and its display is formed by the logical OR with the cursor. The 8th line CGRAM data bits 0 to 4 must be set to "0". If any of the 8th line CGRAM data bits 0 to 4 is set to "1", the corresponding display location will light up regardless of the cursor position.
6. When the Character Code Bits 4 to 7 are set to "0", then the CGRAM Character Pattern is selected. It must be noted that Character Code Bit 3 is not relevant and will not have any effect on the character display. Because of this, the first Character Pattern shown above (R) can be displayed when the Character Code is 00H or 08H.

RELATIONSHIP BETWEEN CGRAM ADDRESS, DDRAM CHARACTER CODE AND CGRAM CHARACTER PATTERNS (FOR 5 X10 DOT CHARACTER PATTERN)

Character Codes (DDRAM Data)									CGRAM Address						Character Patterns (CGRAM Data)								
7	6	5	4	3	2	1	0		5	4	3	2	1	0	7	6	5	4	3	2	1	0	
High						Low			High				Low		High						Low		
0	0	0	0	*	0	0	*		0	0	0	0	0	0	*	*	*	0	0	1	0	0	Character pattern 1
											0	0	0	1	*	*	*	0	1	1	1	0	
											0	0	1	0	*	*	*	1	0	1	0	1	
											0	0	1	1	*	*	*	1	0	1	0	0	
											0	1	0	0	*	*	*	0	1	1	0	0	
											0	1	0	1	*	*	*	0	0	1	1	0	
											0	1	1	0	*	*	*	0	0	1	0	1	
											0	1	1	1	*	*	*	1	0	1	0	1	
											1	0	0	0	*	*	*	0	1	1	1	0	
											1	0	0	1	*	*	*	0	0	1	0	0	
											1	0	1	0	*	*	*	*	*	*	*	*	Cursor Position
											1	0	1	1	*	*	*	*	*	*	*	*	
											1	1	0	0	*	*	*	*	*	*	*	*	
											1	1	0	1	*	*	*	*	*	*	*	*	
											1	1	1	0	*	*	*	*	*	*	*	*	
											1	1	1	1	*	*	*	*	*	*	*	*	
0	0	0	0	*	. . . .	. . . .	*		. . . .	. . . .	. . . .	. . . .	. . . .	. . . .	*	*	*	. . . .	. . . .	. . . .	. . . .	. . . .	Character pattern 2~3
0	0	0	0	*	1	1	*		1	1	0	0	0	0	*	*	*	1	0	1	0	1	Character pattern 4
											0	0	0	1	*	*	*	1	1	1	1	1	
											0	0	1	0	*	*	*	1	1	1	1	1	
											0	0	1	1	*	*	*	1	1	1	1	1	
											0	1	0	0	*	*	*	0	1	1	1	0	
											0	1	0	1	*	*	*	0	0	1	0	0	
											0	1	1	0	*	*	*	0	0	1	0	0	
											0	1	1	1	*	*	*	1	0	1	0	1	
											1	0	0	0	*	*	*	0	1	1	1	0	
											1	0	0	1	*	*	*	0	0	1	0	0	
											1	0	1	0	*	*	*	*	*	*	*	*	Cursor Position
											1	0	1	1	*	*	*	*	*	*	*	*	
											1	1	0	0	*	*	*	*	*	*	*	*	
											1	1	0	1	*	*	*	*	*	*	*	*	
											1	1	1	0	*	*	*	*	*	*	*	*	
											1	1	1	1	*	*	*	*	*	*	*	*	

Notes:

1. * = Not Relevant

2. The character pattern row positions correspond to the CGRAM data bits -- 0 to 4, where bit 4 is in the left position.
3. Character Code Bits 1 and 2 correspond to the CGRAM Address Bits -- 4 and 5 respectively (2 bits : 4 types)
4. If the CGRAM Data is set to "1", then the selection is displayed. If the CGRAM is set to "0", there no selection is made.
5. The CGRAM Address Bits 0 to 3 are used to define the character pattern line position. The 11th line is the cursor position and its display is formed by the logical OR with the cursor. The 11th line CGRAM data bits 0 to 4 must be set to "0". If any of the 11th line CGRAM data bits 0 to 4 is set to "1", the corresponding display location will light up regardless of the cursor position.
6. When the Character Code Bits 4 to 7 are set to "0", then the CGRAM Character Pattern is selected. It must be noted that Character Code Bit -- 0 and 3 are not relevant and will not have any effect on the character display. Because of this, the Character Pattern shown above ($) can be displayed when the Character Code is 00H, 01H, 08H or 09H.

TIMING GENERATION CIRCUIT

The timing signals for the internal circuit operations (i.e. DDRAM, CGRAM, and CGROM) are generated by the Timing Generation Circuit. The timing signals for the MPU internal operation and the RAM Read for Display are generated separately in order to prevent one from interfering with the other. This means that, for example, when the data is being written into the DDRAM, there will be no unwanted interference such as flickering in areas other than the display area.

OLED DRIVER CIRCUIT

WS0010 provides 16 Common Drivers and 100 Segment Driver Outputs. When a character font and the number of lines to be displayed have been selected, the corresponding Common Drivers output the waveform automatically. A non-selection waveform will be outputted by the rest of the Common outputs.

CURSOR/BLINK CONTROL CIRCUIT

The cursor or character blinking is generated by the Cursor / Blink Control Circuit. The cursor or the blinking will appear with the digit located at the Display Data RAM (DDRAM) Address Set in the Address Counter (AC).

	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Address counter	0	0	0	0	1	1	1

CASE 1: FOR 1-LINE DISPLAY

Example: When the Address Counter (AC) is set to 0EH, the cursor position is displayed at DDRAM Address 0EH.

Display position	1	2	3	4	5	**……**	14	15	**……**	19	20
DDRAM address (hexadecimal)	00	01	02	03	04	**……**	0D	**0E**	**……**	12	13

Cursor Position

Note: The cursor or blinking appears when the Address Counter (AC) selects the Character Generator RAM (CGRAM). When the AC selects CGRAM Address, then the cursor or the blinking is displayed in a irrelevant and meaningless position.

CASE 2: FOR 2-LINE DISPLAY

Example: When the Address Counter (AC) is set to 46H, the cursor position is displayed at DDRAM Address 46H.

Display position	1	2	3	4	5	6	7	8	**……**	19	20
DDRAM address	00	01	02	03	04	05	06	07	**……**	09	13
(hexadecimal)	40	41	42	43	44	45	**46**	47	**……**	49	53

Cursor Position

Note:
The cursor or blinking appears when the Address Counter (AC) selects the Character Generator RAM (CGRAM). When the AC selects CGRAM Address, then the cursor or the blinking is displayed in an irrelevant and meaningless position.

INTERNAL RESET CIRCUIT INITIALIZATION

When power is turned ON, WS0010 is initialized automatically by an internal reset circuit . The following items are set (default) during the initialization.

1. Display clear
2. Function set:
   DL="1": 8-bit interface data
   N="0": 1-line display
   F="0": 5 x 8 dot character font

3. Power turn off
   PWR="0"
4. Display on/off control:
   D="0": Display off
   C="0": Cursor off
   B="0": Blinking off
5. Entry mode set
   I/D="0": Decrement by 1
   S="0": No shift

6. Cursor/Display shift/Mode / Pwr
   S/C="0", R/L="1": Shifts cursor position to the right
   G/C="0": Character mode
   Pwr="1": Internal DCDC power on

The Busy Flag (BF) is in a busy state until the initialization is completed (BF="1"). The busy state will be in effect 10 ms after VDD stabilization.

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CHARACTER MODE ADDRESSING

WS0010 provides two kind of character mode. User can fill in 128 characters data (N=0, one line) or 64 characters data per line (N=1, two line) in embedded RAM to display graphic. Character mode address can be controlled by DDRAM address instruction.

Address Format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CA (Character Address)	1	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0

(1)1-Line condition (N=0)

1	2	3	4	……	……	125	126	127	128
CA=10000000	CA=10000001	CA=10000010	CA=10000011	……	……	CA=11111100	CA=11111101	CA=11111110	CA=11111111

(2)2-Line condition (N=1)

1	2	3	4	……	……	61	62	63	64
CA=10000000	CA=10000001	CA=10000010	CA=10000011	……	……	CA=10111100	CA=10111101	CA=10111110	CA=10111111
CA=11000000	CA=11000001	CA=11000010	CA=11000011	……	……	CA=11111100	CA=11111101	CA=11111110	CA=11111111

GRAPHIC MODE ADDRESSING

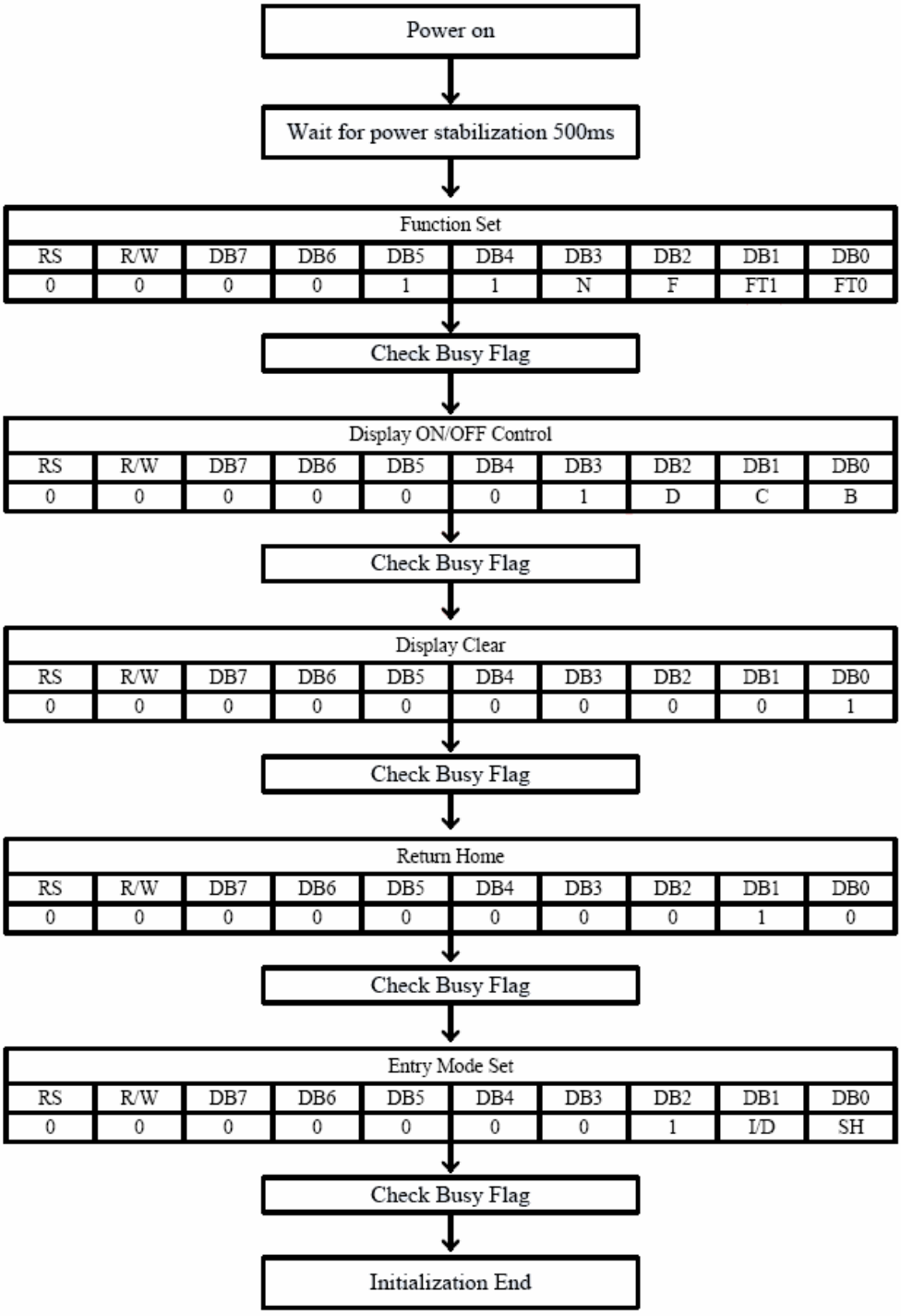
WS0010 provides not only character mode but also graphic mode. User can fill in 100x16 data in embedded RAM to display graphic. Graphic mode addressing is different from character mode.
Use DDRAM address instruction to set X-axis address of Graphic mode and CGRAM address instruction to set Y-axis of Graphic mode.

Address Format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
GXA (Graphic X-axis Address)	1	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
GYA (Graphic Y-axis Address)	0	1	0	0	0	0	0	CGA0

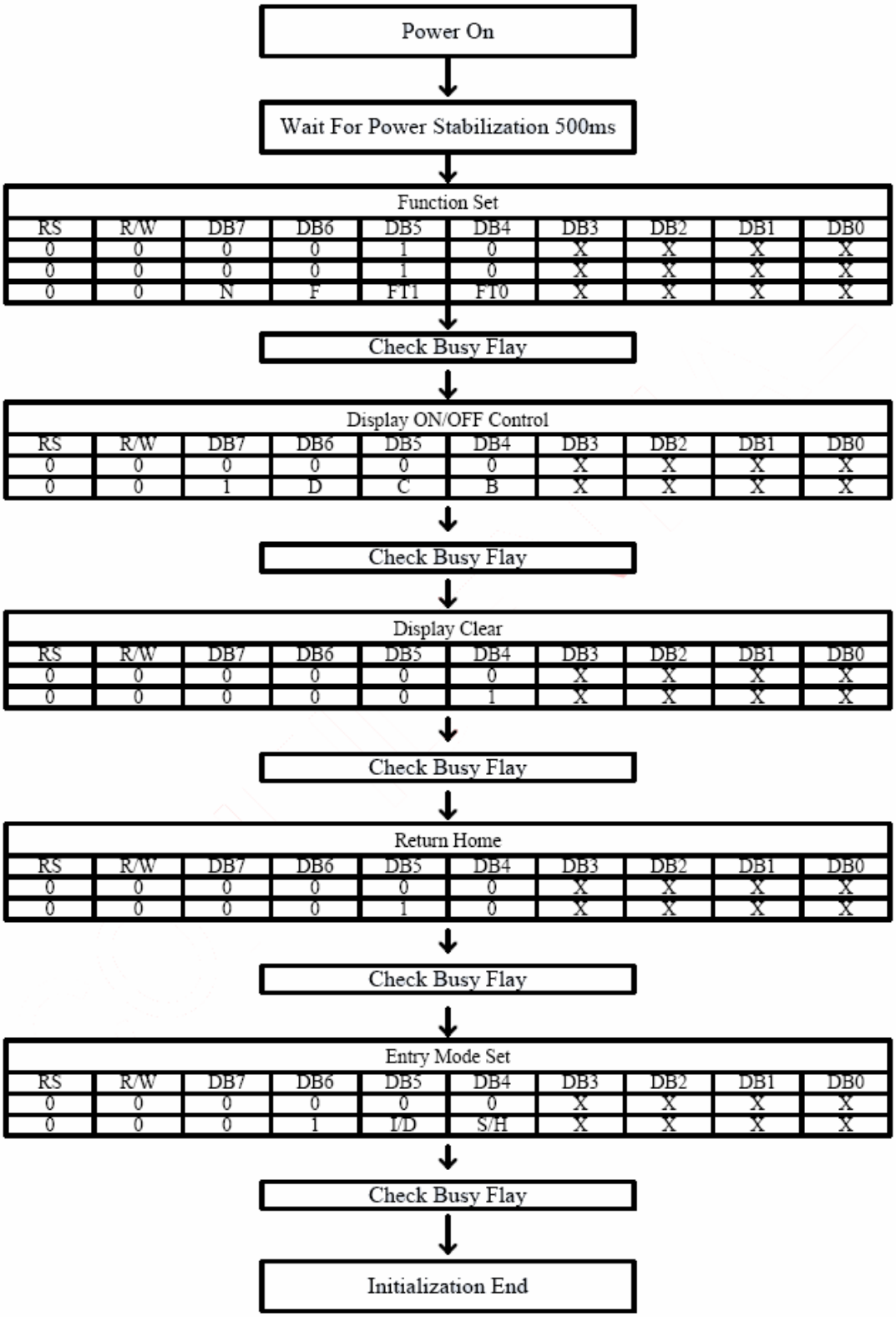
	1	2	3	4	……	……	97	98	99	100
CGA0=0	GXA=10000000 GYA=01000000	GXA=10000001 GYA=01000000	GXA=10000010 GYA=01000000	GXA=10000011 GYA=01000000	D0 D1 D2 D3 D4 D5 D6 D7	……	GXA=11100000 GYA=01000000	GXA=11100001 GYA=01000000	GXA=11100010 GYA=01000000	GXA=11100011 GYA=01000000
CGA0=1	GXA=10000000 GYA=01000001	GXA=10000001 GYA=01000001	GXA=10000010 GYA=01000001	GXA=10000011 GYA=01000001	D0 D1 D2 D3 D4 D5 D6 D7	……	GXA=11100000 GYA=01000001	GXA=11100001 GYA=01000001	GXA=11100010 GYA=01000001	GXA=11100011 GYA=01000001

INITIALIZATION BY INSTRUCTION

(1)8-bit mode



(2)4-bit mode


Power On
Wait For Power Stabilization 500ms
Function Set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 1 0 X X X X
0 0 0 0 1 0 X X X X
0 0 N F FT1 FT0 X X X X
Check Busy Flay
Display ON/OFF Control
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 X X X X
0 0 1 D C B X X X X
Check Busy Flay
Display Clear
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 X X X X
0 0 0 0 0 1 X X X X
Check Busy Flay
Return Home
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 X X X X
0 0 0 0 1 0 X X X X
Check Busy Flay
Entry Mode Set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 X X X X
0 0 0 1 I/D S/H X X X X
Check Busy Flay
Initialization End

INSTRUCTIONS

WS0010's Instruction Register (IR) and Data Register (DR) are the only registers that can be controlled by the MPU. Prior to the commencement of it internal operation, WS0010 temporarily stores the control information to its Instruction Register (IR) and Data Register (DR) in order to easily facilitate interface with various types of MPU. The internal operations of the WS0010 are determined by the signals (RS, R/WB, DB0 to DB7) that are sent from the MPU. These signals are categorized into 4 instructions types, namely:

1. Function Setting Instructions (i.e. Display, Format, Data Length etc.)
2. Internal RAM Address Setting Instructions
3. Data Transfer with Internal RAM Instructions
4. Miscellaneous Function Instructions

The generally used instructions are those that execute data transfers with the internal RAM. However, when the internal RAM addresses are auto incremented/decremented by 1 after each Data Write, the program load of the MPU is lightened. The Display Shift Instruction can be executed at the same time as the Display Data Write, thereby minimizing system development time with maximum programming efficiency.

When an instruction is being executed for an internal operation, only the Busy Flag/Address Read Instruction can be performed. The other instructions are not valid. It should be noted that during the execution of an instruction, the Busy Flag is set to "1". The Busy Flag is set to "0" when the instructions are can be accepted and executed. Therefore, the Busy Flag should be checked to make certain that BF = "0" before sending another instruction from the MPU. If not, the time between the first instruction and the next instruction is longer than the time it takes to execute the instruction itself.

Instruction	Code										Description	Max. Execution Time when fsp or fosc = 250KHz
	RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display.	6.2ms
Return Home	0	0	0	0	0	0	0	0	1	0	Sets DDRAM Address 0 into the Address Counter. Returns shifted display to original position. DDRAM contents remain unchanged. (DB0 is test pin. User should set DB0=0 all the time)	0
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. (These operations are performed during data write and read.)	0
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets entire Display (D) ON/OFF. Sets Cursor (C) ON/OFF. Sets Blinking (B) of Cursor Position Character.	0
Cursor/ Display Shift/ Mode/ Pwr	0	0	0	0	0	1	S/C	R/L	0	0	Moves cursor & shifts display without changing DDRAM contents.	0
							G/C	PWR	1	1	Sets Graphic/Character Mode Sets internal power on/off	
Function Set	0	0	0	0	1	DL	N	F	FT1	FT0	Sets interface data length (DL). Sets number of display lines (N). Sets Character Font (F). Sets Font Table (FT) *Forbids to set FT=01 or 11 when WS0010 be operated in 4-bit interface.	0
Set CGRAM Address	0	0	0	1	ACG	ACG	ACG	ACG	ACG	ACG	Sets CGRAM Address. CGRAM data is sent and received after this setting.	0
Set DDRAM Address	0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD	Sets DDRAM Address. The DDRAM data Is sent and received after this setting.	0
Read Busy Flag & Address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads Busy Flag (BF) indicating that internal operation is being performed. Reads Address Counter contents.	0
Write data into the CGRAM or DDRAM	1	0	Write Data								Writes data into the CGRAM or DDRAM	0
Read Data from the CGRAM or DDRAM	1	1	Read Data								Read data from the CGRAM or DDRAM	0

Notes:

1. After the CGRAM/DDRAM Read or Write Instruction has been executed, the RAM Address Counter is incremented or decremented by 1. After the Busy Flag is turned OFF, the RAM Address is updated.
2. I/D=Increment/Decrement Bit
   - I/D="1": Increment
   - I/D="0": Decrement
3. S=Shift Entire Display Control Bit. When S=”0”, shift function disable.
4. BF=Busy Flag
   - BF="1": Internal Operating in Progress
   - BF="0": No Internal Operation is being executed, next instruction can be accepted.
5. R/L=Shift Right/Left
   - R/L="1": Shift to the Right
   - R/L="0": Shift to the Left
6. S/C=Display Shift/Cursor Move
   - S/C="1": Display Shift
   - S/C="0": Cursor Move
7. G/C=Graphic/Character mode selection. G/C=”0”, Character mode is selected. G/C=”1”, Graphic mode is selected.
8. PWR=Internal DCDC on/of control. PWR=”1”, DCDC on. PWR=”0”, DCDC off.
9. DDRAM=Display Data RAM
10. CGRAM=Character Generator RAM
11. ACG=CGRAM Address
12. ADD=Address Counter Address (corresponds to cursor address)
13. AC=Address Counter (used for DDRAM and CGRAM Addresses)
14. F=Character Pattern Mode
    - F="1": 5 x 10 dots
    - F="0": 5 x 8 dots
15. N=Number of Lines Displayed
    - N="1": 2 -Line Display
    - N="0": 1-Line Display

INSTRUCTION DESCRIPTION

CLEAR DISPLAY INSTRUCTION

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

This instruction is used to clear the Display Write Space 20H in all DDRAM Addresses. That is, the character pattern for the Character Code 20H must be a BLANK pattern. It then sets the DDRAM Address 0 into the Address Counter and reverts the display to its original state (if the display has been shifted). The display will be cleared and the cursor or blinking will go to the left edge of the display. If there are 2 lines displayed, the cursor or blinking will go to the first line 's left edge of the display. Under the Entry Mode, this instruction also sets the I/D to 1 (Increment Mode). The S Bit of the Entry Mode does not change.

RETURN HOME INSTRUCTION

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	*

Note: * = Not Relevant

This instruction is used to set the DDRAM Address 0 into the Address Counter and revert the display to its original status (if the display has been shifted). The DDRAM contents do not change.
The cursor or blinking will go to the left edge of the display. If there are 2 lines displayed, the cursor or blinking will go to the first line's left edge of the display.

ENTRY MODE SET INSTRUCTION

The Entry Mode Set Instruction has two controlling bits: I/D and S. Please refer to the table below.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

I/D IS THE INCREMENT/DECREMENT BIT.

When I/D is set to "1", the DDRAM Address is incremented by "1" when a character code is written into or read from the DDRAM. An increment of 1 will move the cursor or blinking one step to the right.

When I/D is set to "0", the DDRAM is decremented by 1 when a character code is written into or read from the DDRAM. A decrement of 1 will move the cursor or blinking one step to the left.

S: SHIFT ENTIRE DISPLAY CONTROL BIT

This bit is used to shift the entire display. When S is set to "1", the entire display is shifted to the right (when I/D ="0") or left (when I/D ="1"). When S is set to "0", the display is not shifted.

Ex1 : I/D=1, S=1

		1	2	3	4	_	Initial display
	1	2	3	4	A	_	Input new character "A"
1	2	3	4	A	B	_	Input new character "B"
2	3	4	A	B	C	_	Input new character "C"
3	4	A	B	C	D	_	Input new character "D"

Ex2 : I/D=0, S=1

1	2	3	4	_			Initial display
	1	2	3	4	A		Input new character "A"
		1	2	3	B	A	Input new character "B"
			1	2	C	B	Input new character "C"
				1	D	C	Input new character "D"

DISPLAY ON/OFF CONTROL INSTRUCTION

The Display On / OFF Instruction is used to turn the display ON or OFF. The controlling bits are D, C and B.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

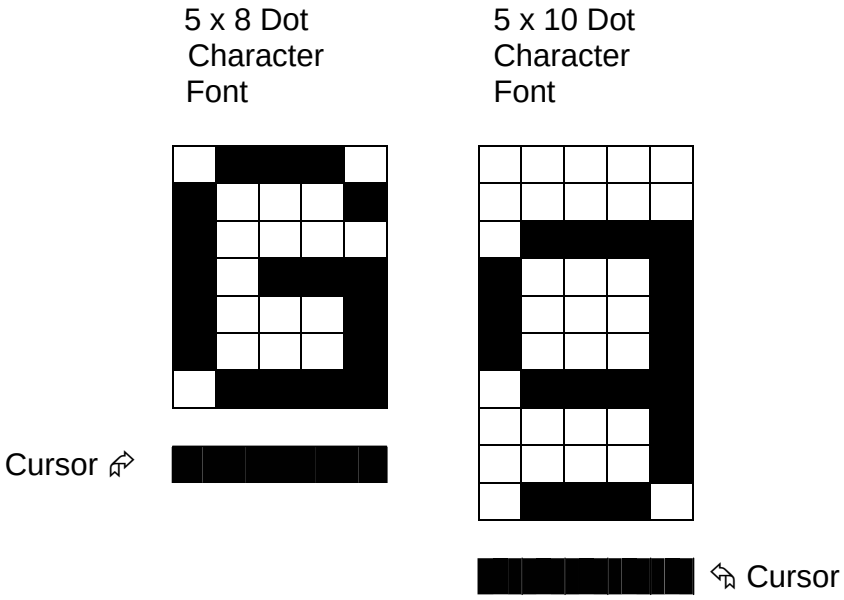
D: DISPLAY ON/OFF BIT

When D is set to "1", the display is turned ON. When D is set to "0", the display is turned OFF and the display data is stored in the DDRAM. The display data can be instantly displayed by setting D to "1".

C: CURSOR DISPLAY CONTROL BIT

When C is set to "1", the cursor is displayed. In a 5 x 8 dot character font, the cursor is displayed via the 5 dots in the 8th line. In a 5 x 10 dot character font, it is displayed via 5 dots in the 11th line.

When C is set to "0", the cursor display is disabled.
During a Display Data Write, the function of the I/D and others will not be altered even if the cursor is not present. Please refer to the figure below.



B: BLINKING CONTROL BIT

When B is set to '1", the character specified by the cursor blinks. The blinking feature is displayed by switching between the blank dots and the displayed character at a speed of 409.6ms intervals when the fcp or fosc is 250kHz. Please refer to the figure below.

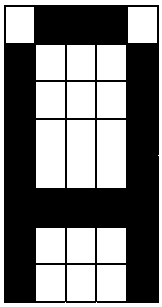


Figure 1

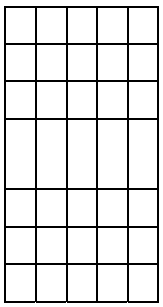


Figure 2

Note: Figures 1 and 2 are alternately displayed

The cursor and the blinking can be set to display at the same time. The blinking frequency depends on the fosc or the reciprocal of fcp.

To illustrate, when fosc=250K Hz, then, the blinking frequency=409.6 x 250/270=379.2ms

CURSOR/DISPLAY SHIFT INSTRUCTION

This instruction is used to shift the cursor or display position to the left or right without writing or reading the Display Data. This function is used to correct or search the display. Please refer to the table below.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	0	0
0	0	0	0	0	1	G/C	PWR	1	1

S/C	R/L	Shift Function
0	0	Shifts the cursor position to the left. (AC is decremented by 1).
0	1	Shifts cursor position to the right. (AC incremented by 1).
1	0	Shifts entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

In a 2-line Display, the cursor moves to the second line when it passes the 40th digit of the first line. The first and second line displays will shift at the same time.

When the displayed data is shifted repeatedly, each line moves only horizontally. The second line display does not shift into the first line position.

The Address Counter (AC) contents will not change if the only action performed is a Display Shift.

G/C: GRAPHIC MODE / CHARACTER MODE SELECTION

This bit is used to select the display mode for further process.
When G/C = 1, the *GRAPHIC MODE* will be selected.
When G/C = 0, the *CHARACTER MODE* will be selected.

PWR: ENABLE/DISABLE INTERNAL POWER

This bit is used to turn ON or turn OFF the internal power.
When PWR = 1, the internal power is turned ON.
When PWR = 0, the internal power is turned OFF.

FUNCTION SET INSTRUCTION

The Function Set Instruction has three controlling 3 bits, namely: DL, N and F. Please refer to the table below.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	FT1	FT0

DL: INTERFACE DATA LENGTH CONTROL BIT

This is used to set the interface data length. When DL is set to "1", the data is sent or received in 8-bit

length via the DB0 to DB7 (for an 8-Bit Data Transfer). When DL is set to "0", the data is sent or received in 4-bit length via DB4 to DB7 (for a 4-Bit Data Transfer). When the 4-bit data length is selected, the data must be sent or received twice.
The default data length is 8-bit, if chip want to operation in 4-Bit interface, the first instruction after power on, set to DL is “0” use function set command and data length is changed from 8-Bit to 4-Bit, secondly, it requires two times (4-Bit twice) to accomplish complete function set command to set DL(4-bit data length), N(display line), F(character font) and FT(font table). 4-Bit operation setting flow please refer to page 28.

N: NUMBER OF DISPLAY LINE

This is used to set the number of display lines. When N="1", the 2-line display is selected. When N is set to "0", the 1-line display is selected.

F: CHARACTER FONT SET

This is used to set the character font set. When F is set to "0", the 5 x 8 dot character font is selected. When F is set to "1", the 5 x 10 dot character font is selected.

It must be noted that the character font setting must be performed at the head of the program before executing any instructions other than the Busy Flag and Address Instruction. Otherwise, the Function Set Instruction cannot be executed unless the interface data length is changed.

FT1, FT0: FONT TABLE SELECTION

These two bits are used to select one font table out of the three for further process.
When (FT1, FT0) = (0, 0), the *ENGLISH_JAPANESE CHARACTER FONT TABLE* will be selected.
(FT1, FT0) = (0, 1), the *WESTERN EUROPEAN CHARACTER FONT TABLE-I* will be selected.
(FT1, FT0) = (1, 0), the *ENGLISH_RUSSIAN CHARACTER FONT TABLE* will be selected.
(FT1, FT0) = (1, 1), the *WESTERN EUROPEAN CHARACTER FONT TABLE-II* will be selected.
Note: The default setting for FT1 and FT0 is 0 and 0 respectively which means the default Font Table is *ENGLISH_JAPANESE CHARACTER FONT TABLE.*

It must be noted that Function Set instruction be executed on display off status.

SET CGRAM ADDRESS INSTRUCTION

This instruction is used to set the CGRAM Address binary AAAAAA into the Address Counter. Data is then written to or read from the MPU for CGRAM.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	ACG	ACG	ACG	ACG	ACG	ACG

Note: ACG is the CGRAM Address

SET DDRAM ADDRESS INSTRUCTION

This instruction is used to set the DDRAM Address binary AAAAAAA into the Address Counter. The data is written to or read from the MPU for the DDRAM. If 1-line display is selected (N="0"), then AAAAAAA can be 00H to 4FH. When the 2-line display is selected, then AAAAAAA can be 00H to 27H for the first line and 40H to 67H for the second line.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD

Note: ADD = DDRAM Address

READ BUSY FLAG AND ADDRESS INSTRUCTION

This instruction is used to read the Busy Flag (BF) to indicate if WS0010 is internally operating on a previously received instruction. If BF is set to "1", then the internal operation is in progress and the next instruction will not be accepted. If the BF is set to "0", then the previously received instruction has been executed and the next instruction can be accepted and processed. It is important to check the BF status before proceeding to the next write operation. The value of the Address Counter in binary AAAAAAA is simultaneously read out. This Address Counter is used by both the CGRAM and the DDRAM and its value is determined by the previous instruction. The contents of the address are the same as for the instructions -- Set CGRAM Address and Set DDRAM Address.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC	AC	AC	AC	AC	AC	AC

Notes:
1. BF=Busy Flag
2. AC=Address Counter

WRITE DATA TO **CGRAM / DDRAM INSTRUCTION**

This instruction writes 8-bit binary data -- DDDDDDDD to the CGRAM or the DDRAM. The previous CGRAM or DDRAM Address setting determines whether a data is to be written into the CGRAM or the DDRAM. After the write process is completed, the address is automatically incremented or decremented by 1 in accordance with the Entry Mode instruction. It must be noted that the Entry Mode instruction also determines the Display Shift.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D	D	D	D	D	D	D	D

READ DATA FROM THE CGRAM OR DDRAM INSTRUCTION

This instruction reads the 8-bit binary data -- DDDDDDDD from the CGRAM or the DDRAM. The Set CGRAM Address or Set DDRAM Address Set Instruction must be executed before this instruction can be performed, otherwise, the first Read Data will not be valid.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D	D	D	D	D	D	D	D

When the Read Instruction is executed in series, the next address data is normally read from the Second Read. There is no need for the Address Set Instruction to be performed before this Read instruction when using the Cursor Shift Instruction to shift the cursor (Reading the DDRAM). The Cursor Shift Instruction has the same operation as that of the Set the DDRAM Address Instruction.

After a Read instruction has been executed, the Entry Mode is automatically incremented or decremented by 1. It must be noted that regardless of the Entry Mode, the Display Shift is not executed.

After the Write instruction to either the CGRAM or DDRAM has been performed, the Address Counter is automatically increased or decreased by 1. The RAM data selected by the Address Counter cannot be read out at this time even if the Read Instructions are executed. Therefore, in order to correctly read the data, the following procedure has suggested:

1. Execute the Address Set or Cursor Shift (only with DDRAM) Instruction
2. Just before reading the desired data, execute the Read Instruction from the second time the Read Instruction has been sent.

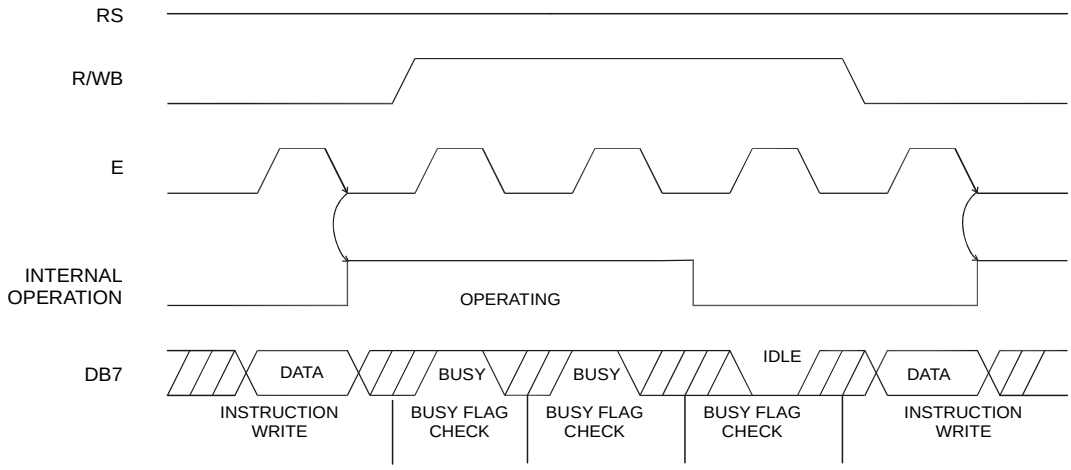
MPU INTERFACE

WS0010 provides High-speed 8-bit parallel bi-directional interface with 6800-series or 8080-series and serial interface. User can choice by signal “PS” and “C68”.

68 – series interface

(a) 8-BIT mode(Not available for serial mode)

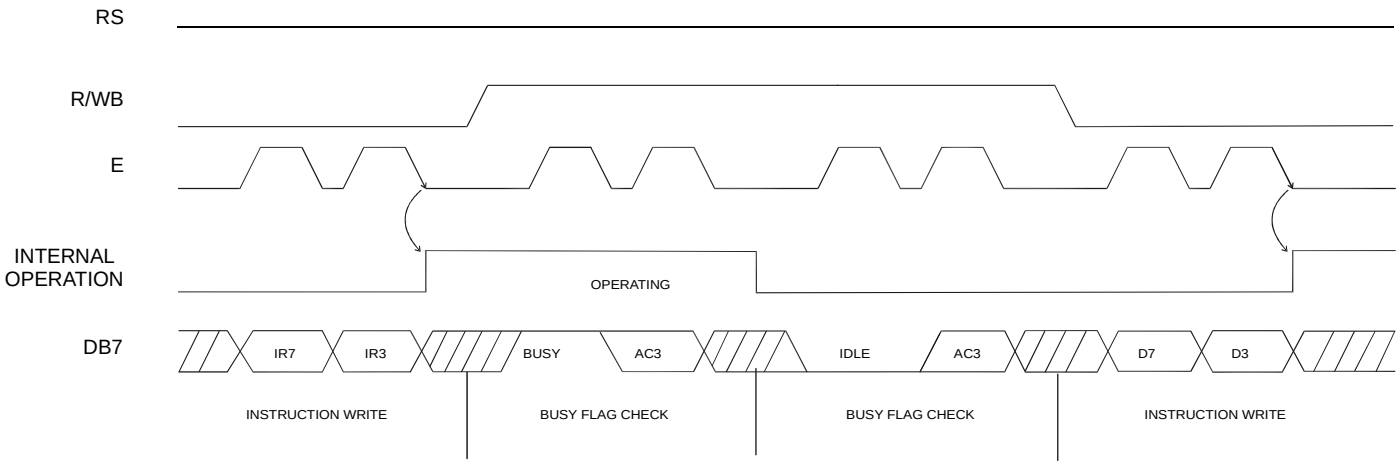
When WS0010 interfaces with an 8-bit MPU, DB0 to DB7 are used. The 8-bit data transfer starts from the four high order bits --DB4 to DB7 followed by the four low order bits -- DB0 to DB3.
An example of a Busy Flag Check Timing in an 8-Bit MPU Interface is given in the diagram below.



(b) 4-BIT mode (Not available for serial mode)

WS0010 can be configured to interface with a 4-bit MPU and is selected via a program. If the I/O port of the 4-Bit MPU from which WS0010 is connected to, is capable of transferring 8 bits, then an 8-bit data transfer operation is executed. Otherwise, two 4-bit data transfer operations are needed to satisfy one complete data transfer.

Under the 4-bit data transfer, DB4 to DB7 are used as bus lines. DB0 to DB3 are disabled. The data transfer between WS0010 and MPU is completed after two 4-bit data have been transferred. The Busy Flag must be checked (one instruction) after completion of the data transfer (that is, 4-bit data has been transferred twice.). The Busy Flag must be checked after two 4-bits data transfer has been completed. Please refer to the diagram below for a 4-bit data transfer timing sequence.



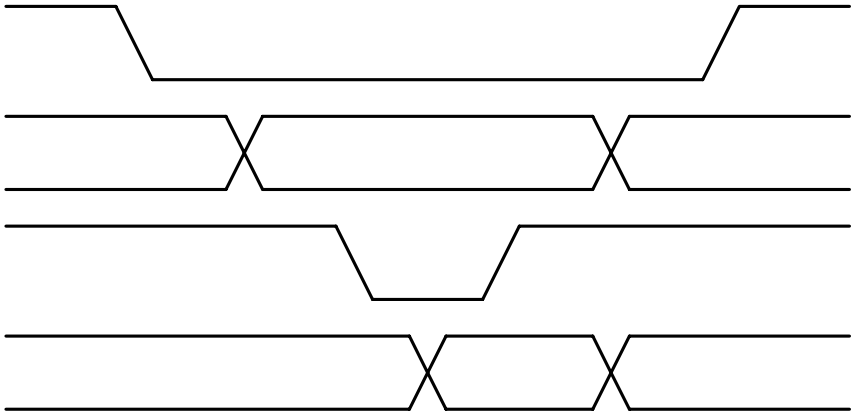
where:

1. IR7=Instruction Bit 7
2. IR3=Instruction Bit 3
3. AC3=Address Counter 3

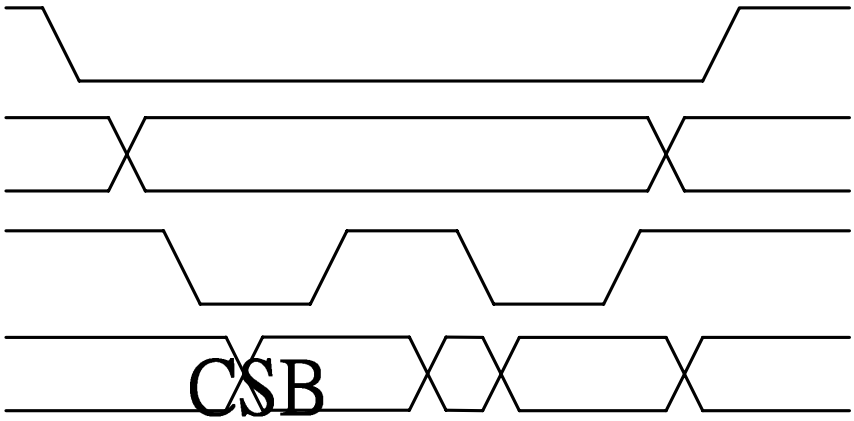
From the above timing diagram, it is important to note that the Busy Flag Check and the data transfer are both executed twice.

80 – series interface

(a) 8-BIT mode



(b) 4-BIT mode

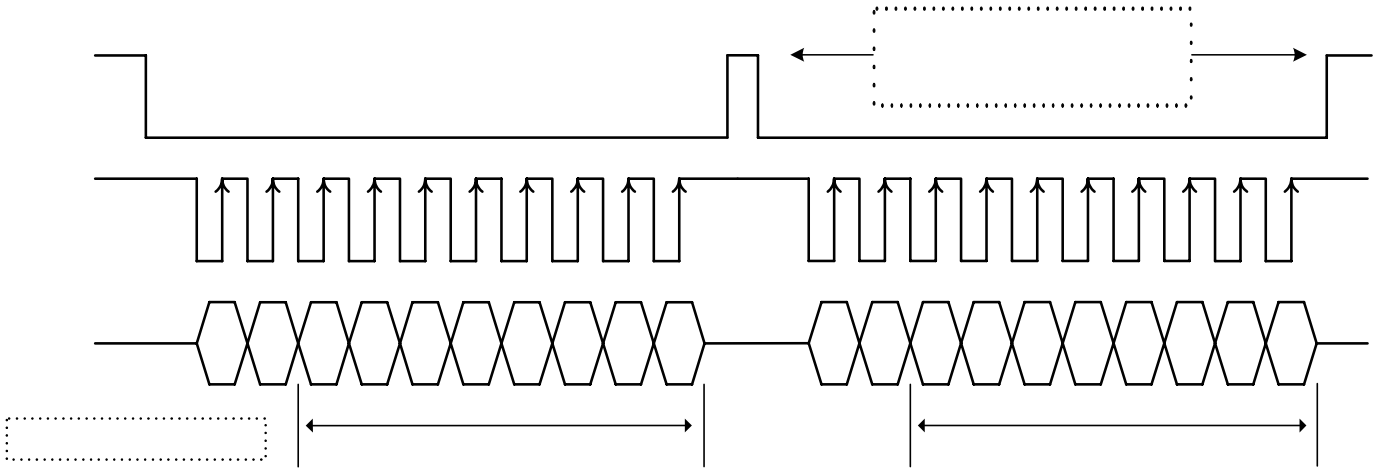


RS

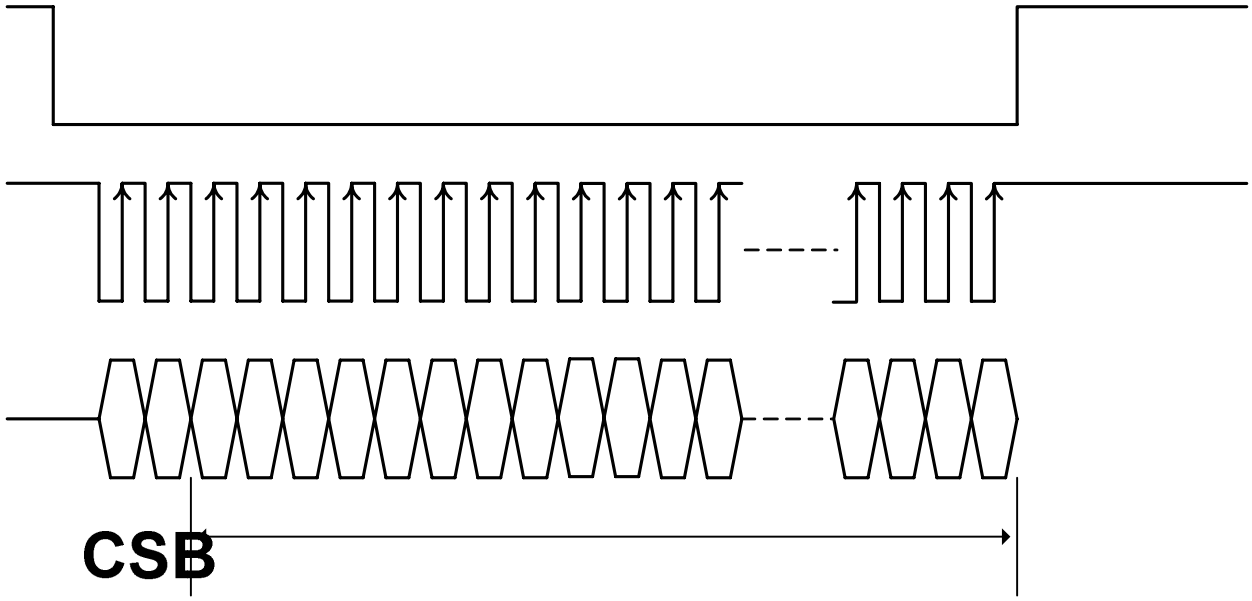
Serial interface

3-line serial write cycle

(a) Command write / RAM data single write



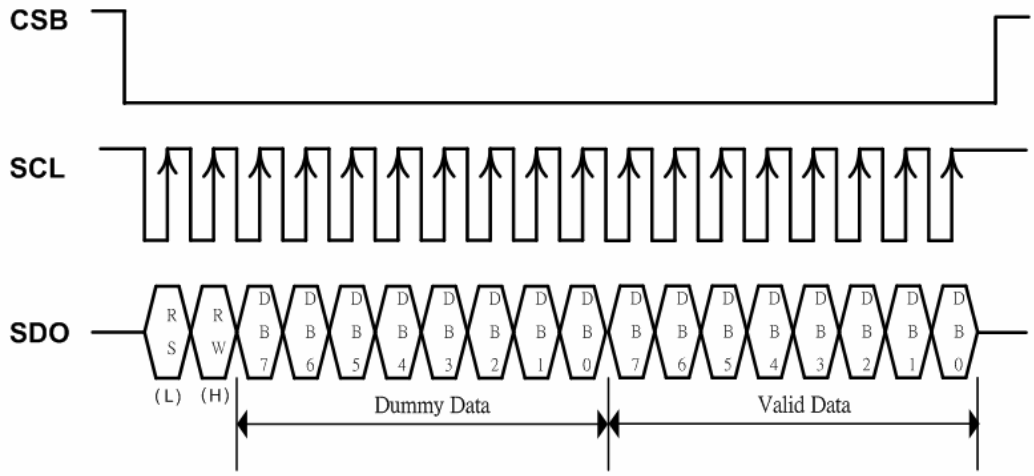
(b) RAM data continuous write



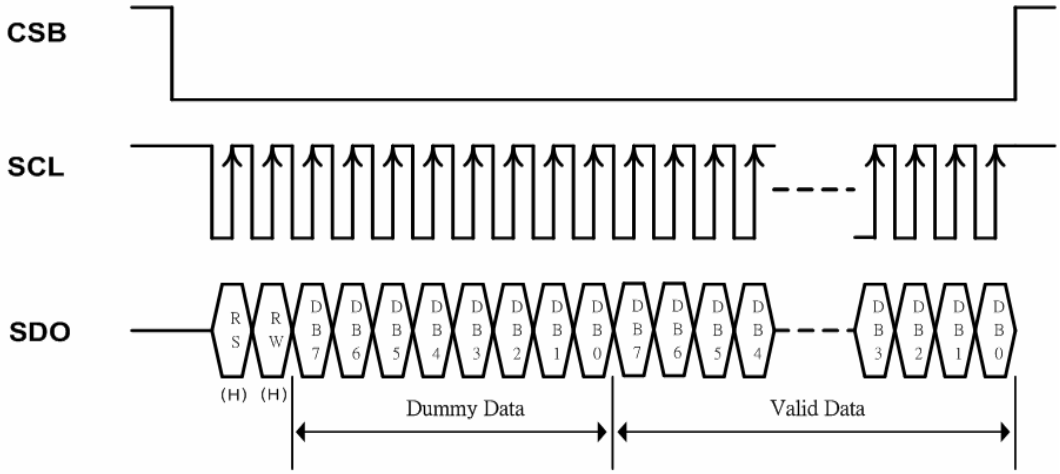
SCL

3-line serial read cycle

(a) Command Read



(b) RAM Read



(a) OLED INTERFACE

WS0010 supports two display types, namely: 5 x 8 dots and 5 x 10 dots character fonts. Each of these types includes a cursor display. Up to 2 lines may be displayed in a 5x 8 dot character font type and 1 line for a 5 x 10 dots character font type. The number of lines that can be displayed as well as the type of font can be selected by using the software program. Please refer to the table below

Number of Display Line	Character Font Type	Number of Common Signals	Duty Factor
1	5 x 8 dots + cursor	8	1/8
1	5 x 10 dots + cursor	11	1/11
2	5 x 8 dots + cursor	16	1/16

As shown in the table above, three types of common signals are available. An example of each configuration is shown in the examples below. It should be noted that every 5 segment signal lines can display one digit, therefore, WS0010 can display up to 8 digits in a 1-line display and 16 digits in a 2-line display.

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)

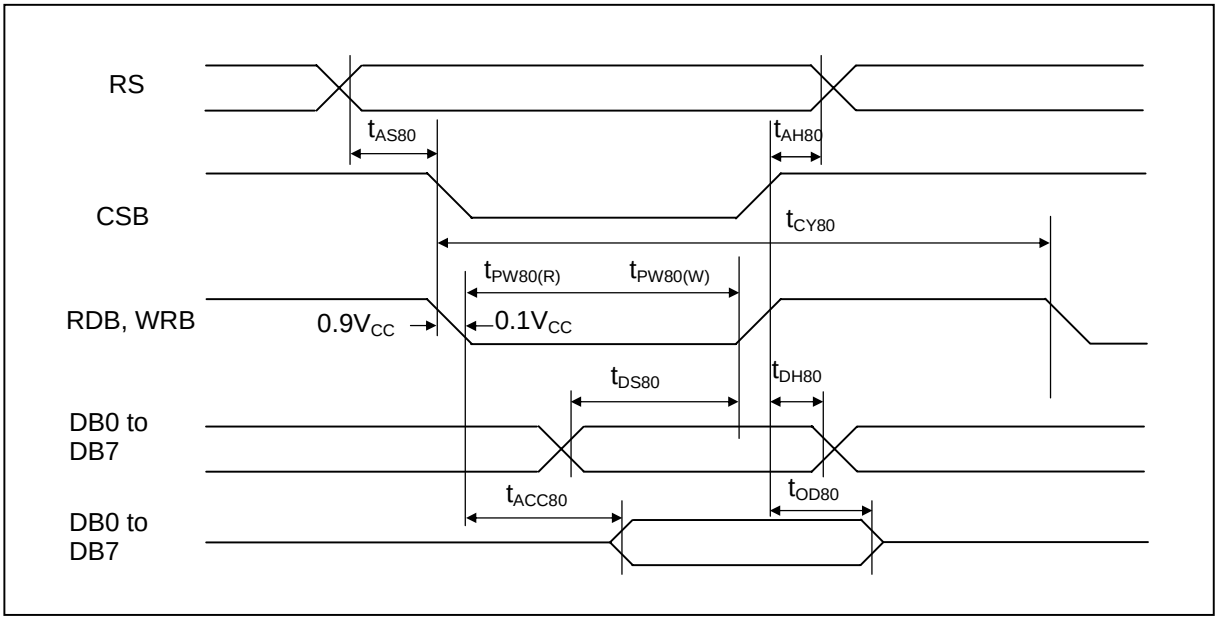


Figure 1. Read / Write Characteristics (8080-series MPU)

(V_{CC} = 3.0 to 5.3V, Ta = -40 to +80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS80} t_{AH80}	20 0	-	-	ns	
System cycle time		t_{CY80}	500	-	-	ns	
Pulse width (WRB)	RW_WRB	t_{PW80}(W)	250	-	-	ns	
Pulse width (RDB)	E_RDB	t_{PW80}(R)	250	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t_{DS80} t_{DH80}	40 20	-	-	ns	
Read access time Output disable time		t_{ACC80} t_{OD80}	- 10	-	180 -	ns	C_L = 100pF

Read / Write Characteristics (6800-series Microprocessor)

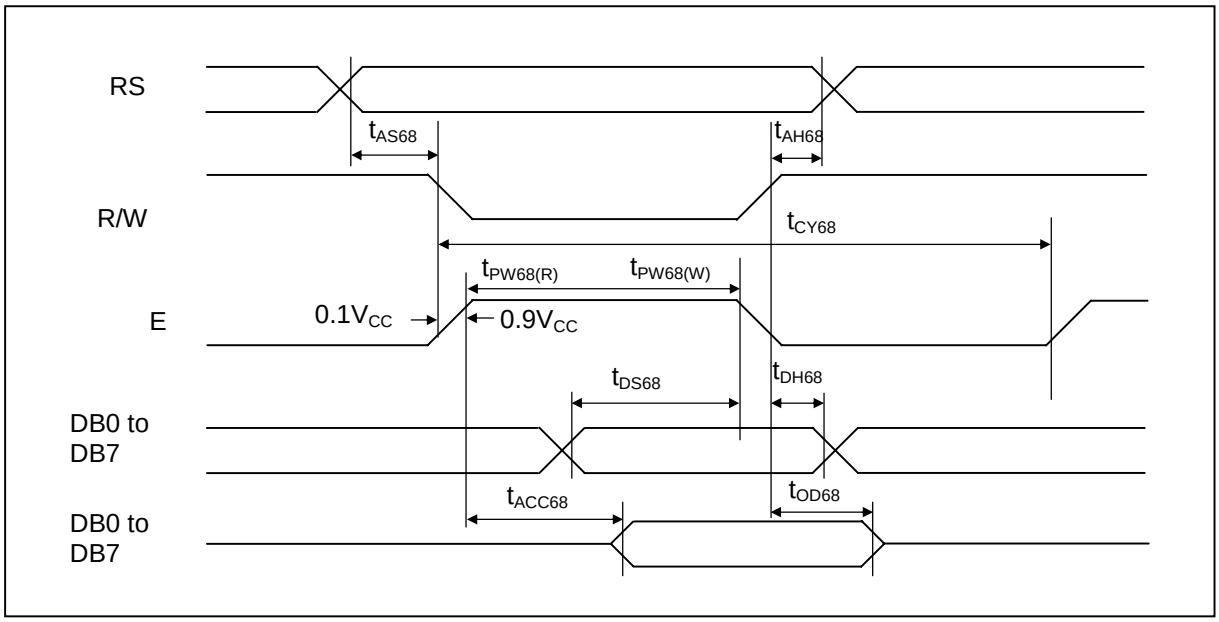


Figure 2. Read / Write Characteristics (6800-series MPU)

(V**cc** = 3.0 to 5.3V, Ta = -40 to +80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t**AS68** t**AH68**	20 0	-	-	ns	
System cycle time		t**CY68**	500	-	-	ns	
Pulse width (E)	E_RDB	t**PW68**(W)	250	-	-	ns	
Pulse width (E)	E_RDB	t**PW68**(R)	250	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t**DS68** t**DH68**	40 20	-	-	ns	
Read access time Output disable time		t**ACC68** t**OD68**	- 10	-	180 -	ns	C**L** = 100pF

Serial Interface Characteristics

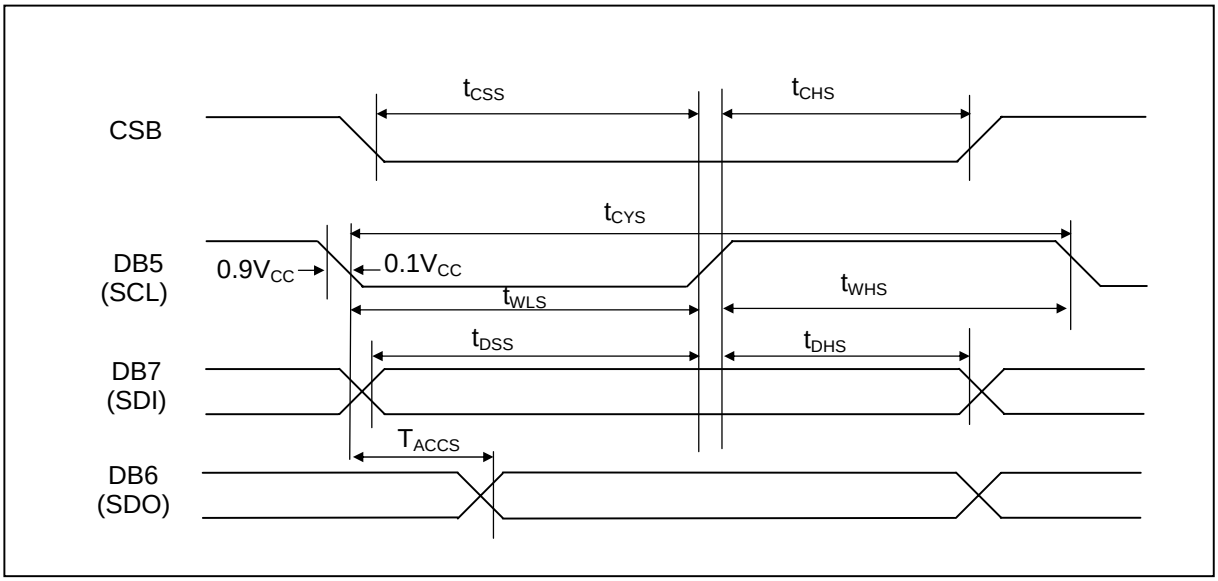


Figure 3. Serial Interface Characteristics

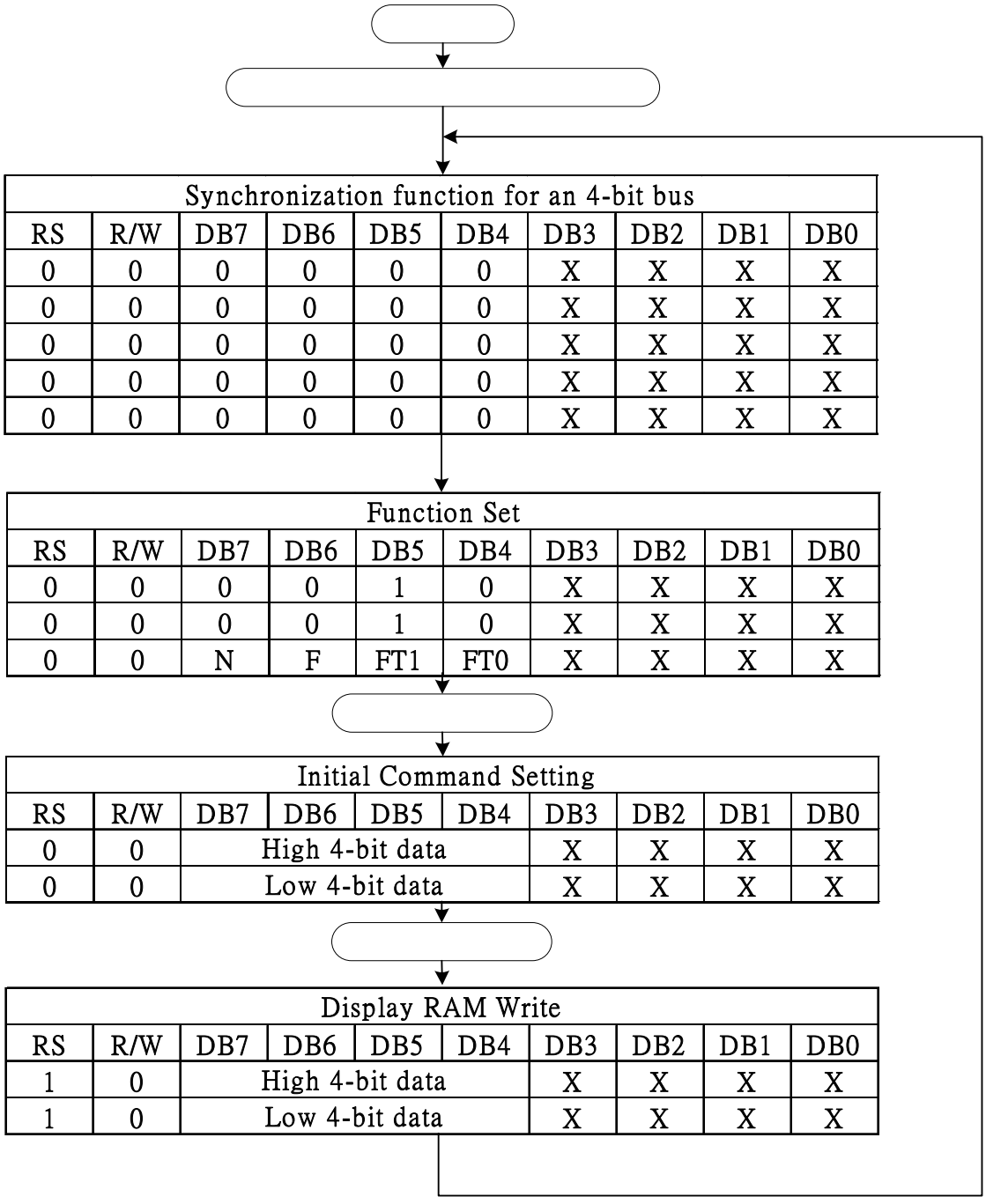
(V**cc** = 3.0 to 5.3V, Ta = -40 to +80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCL high pulse width SCL low pulse width	DB5 (SCL)	t**CYS** t**WHS** t**WLS**	300 100 100	- - -	- - -	ns	
CSB setup time CSB hold time	CSB	t**CSS** t**CHS**	150 150	- -	- -	ns	
Data setup time Data hold time	DB7 (SDI)	t**DSS** t**DHS**	100 100	- -	- -	ns	
Read access time	DB6 (SDO)	t**ACCS**	-	-	80	ns	

Notes

Repeated procedures for an 4-bit bus interface

Noise causing transfer mismatch between the four upper and lower bits can be corrected by a reset triggered by consecutively writing a “0000” instruction five times. The next transfer starts from the lower four bits and then first instruction “Function set” can be executed normally.
Please insert the synchronization function in the head of procedures. The repeated procedures are show as follows :



Synchronization function for an 4-bit bus									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	0	0	0	X	X	X	X
0	0	0	0	0	0	X	X	X	X
0	0	0	0	0	0	X	X	X	X
0	0	0	0	0	0	X	X	X	X

Function Set									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	X	X	X	X
0	0	0	0	1	0	X	X	X	X
0	0	N	F	FT1	FT0	X	X	X	X

Initial Command Setting									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	High 4-bit data				X	X	X	X
0	0	Low 4-bit data				X	X	X	X

Display RAM Write									
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	High 4-bit data				X	X	X	X
1	0	Low 4-bit data				X	X	X	X